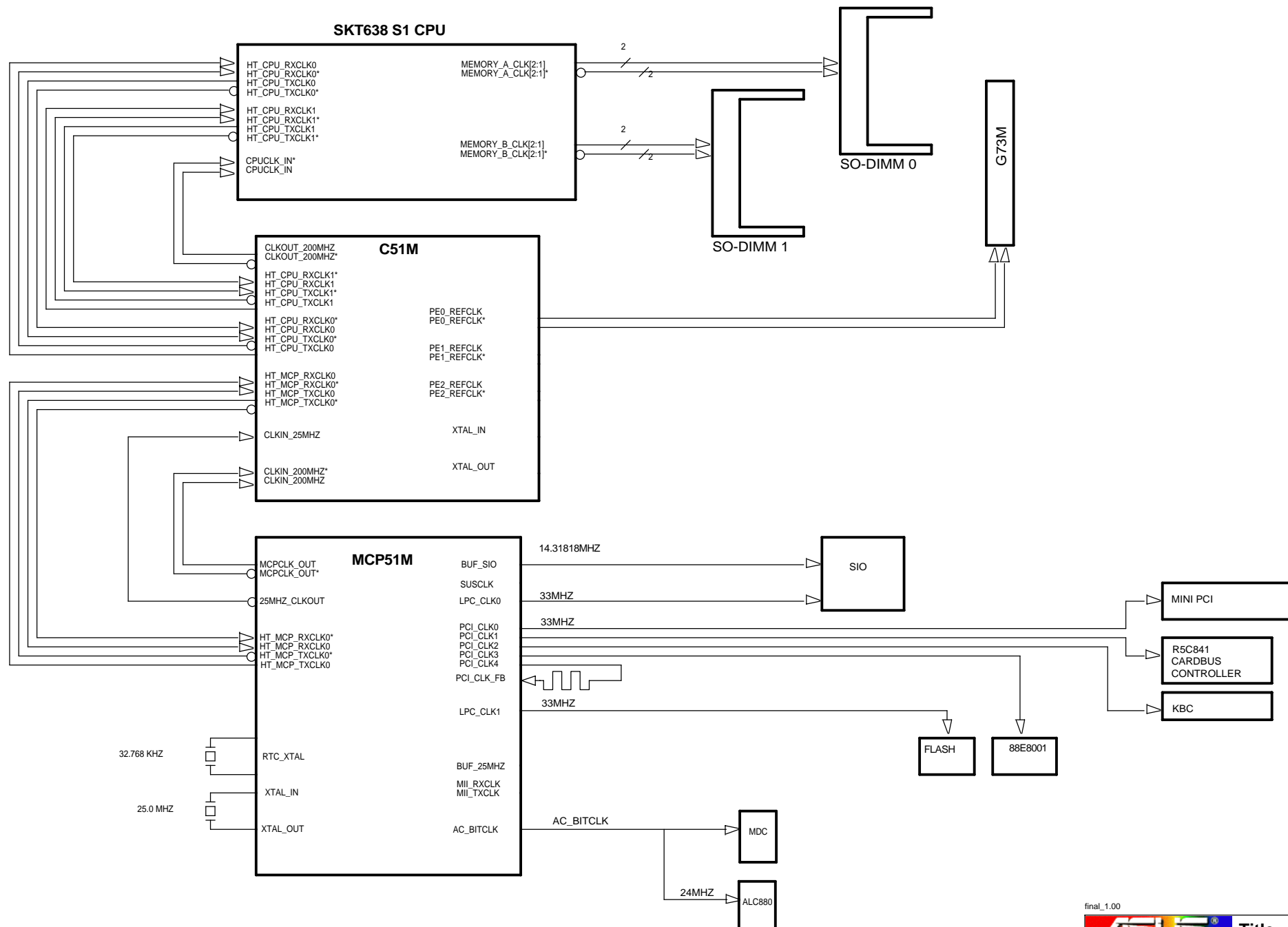


- D

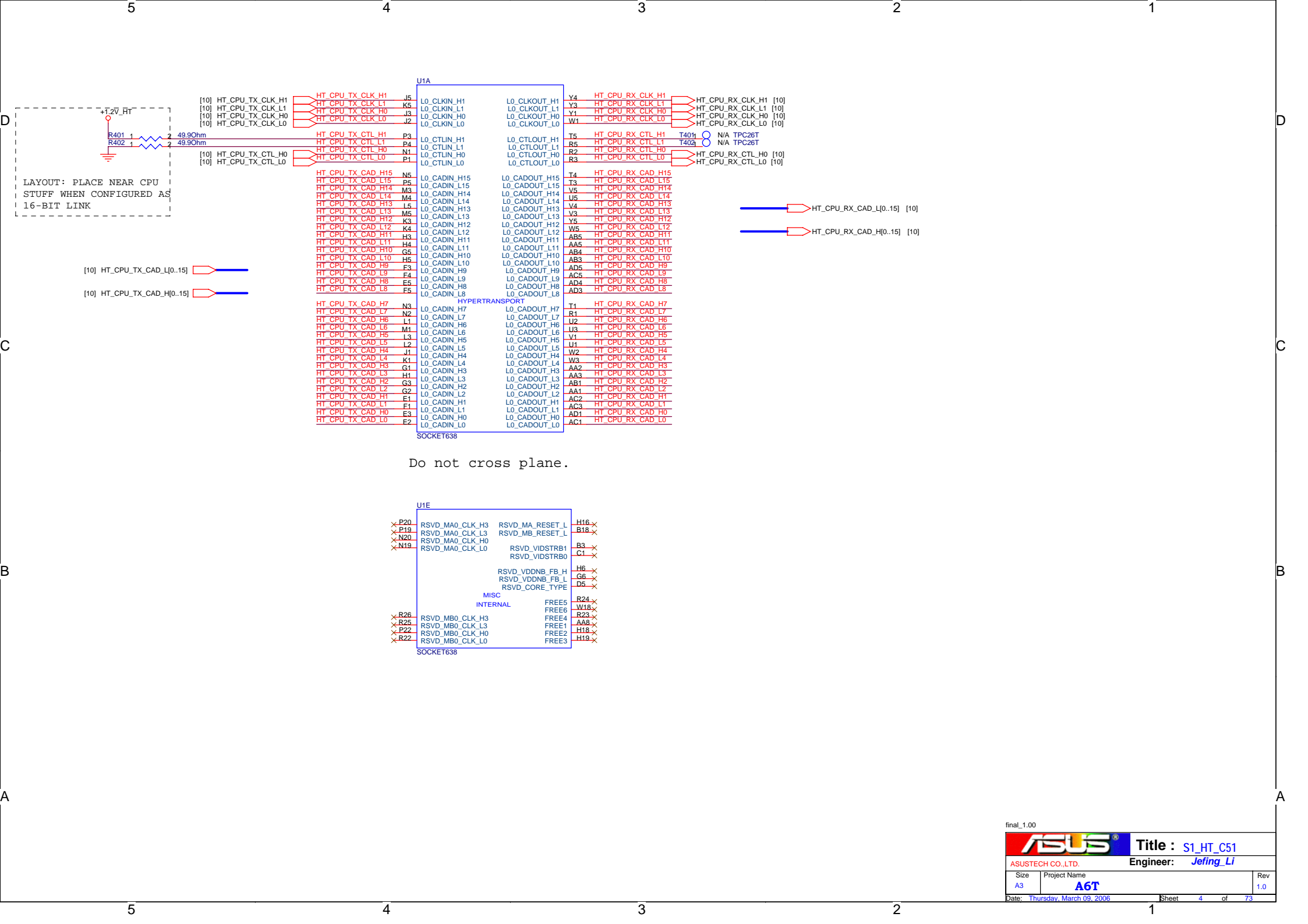


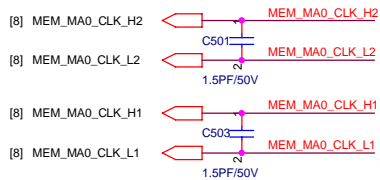
CLOCK MAP



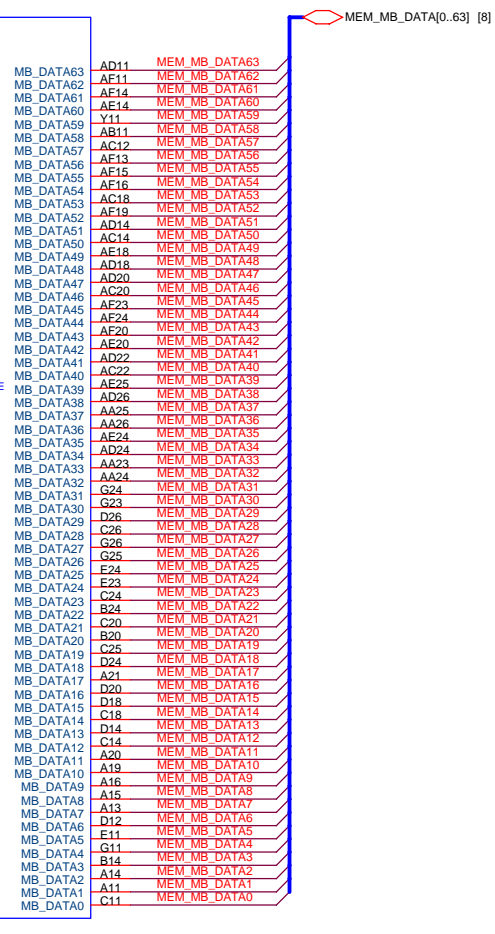
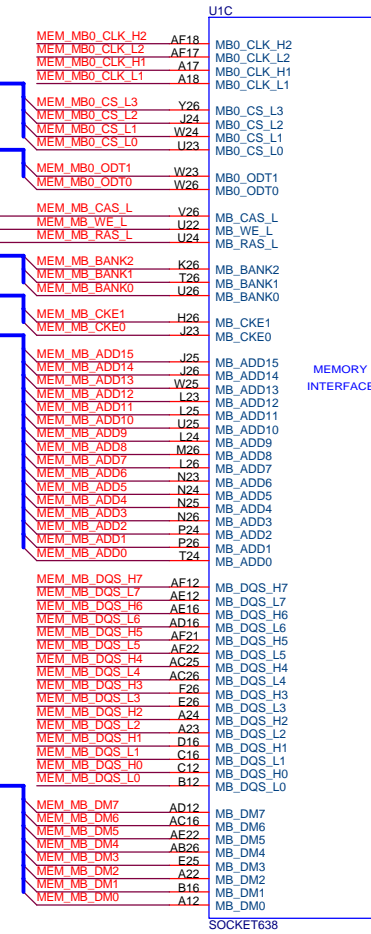
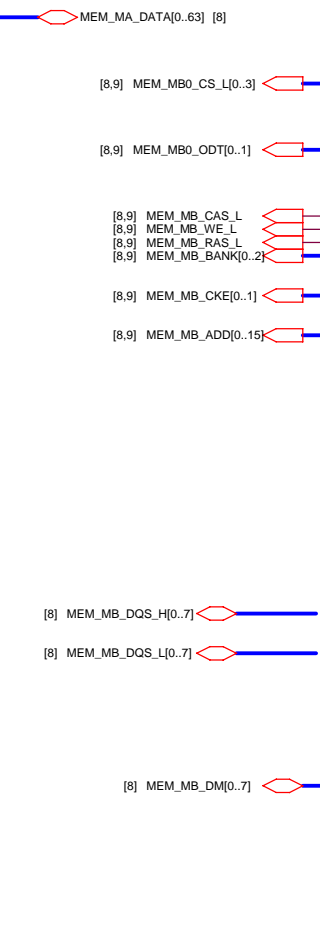
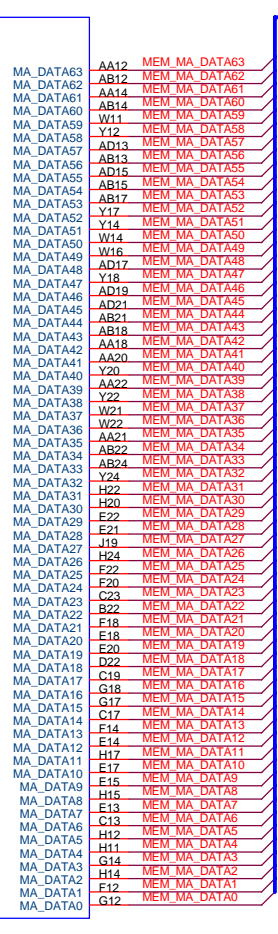
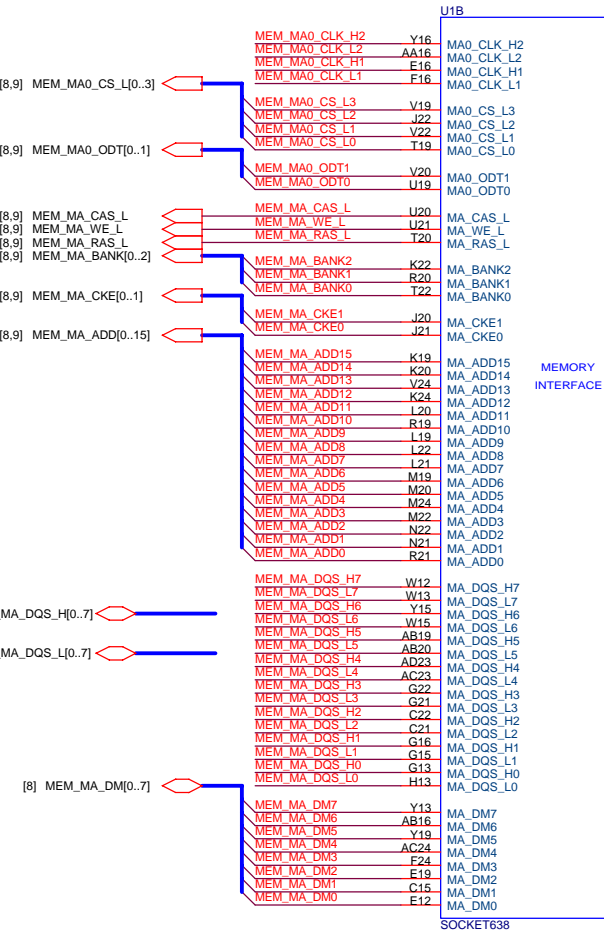
final_1.00

ASUS		Title : CLOCK MAP	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size A3	Project Name A6T	Rev 1.0	Date: Monday, March 06, 2006
Sheet 3 of 73		1	

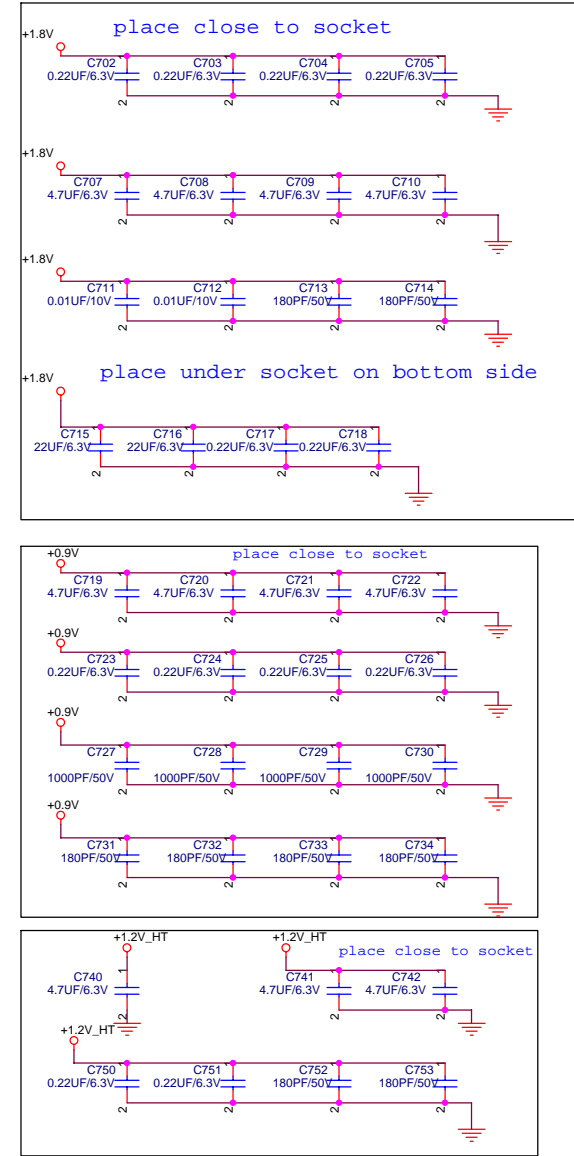
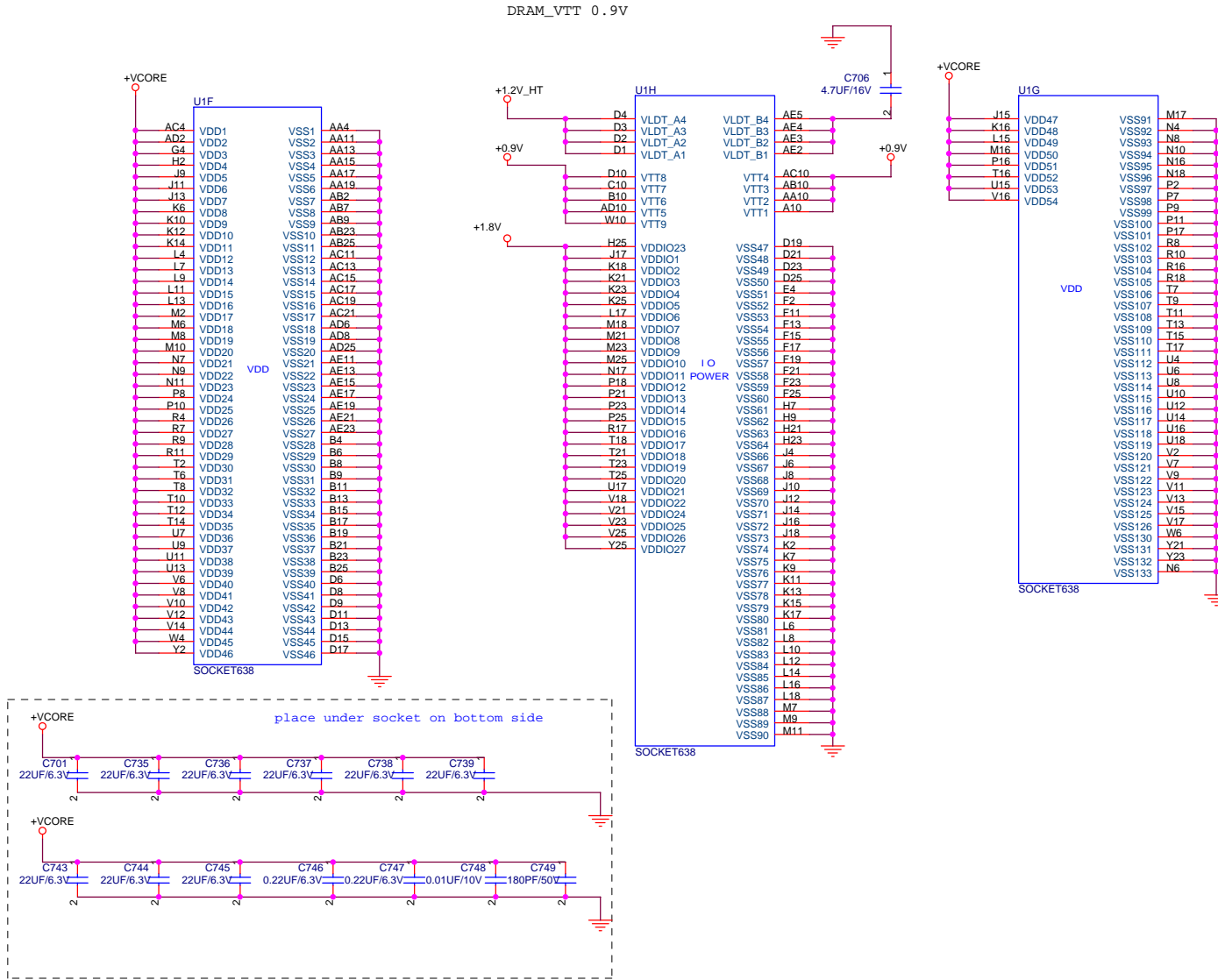


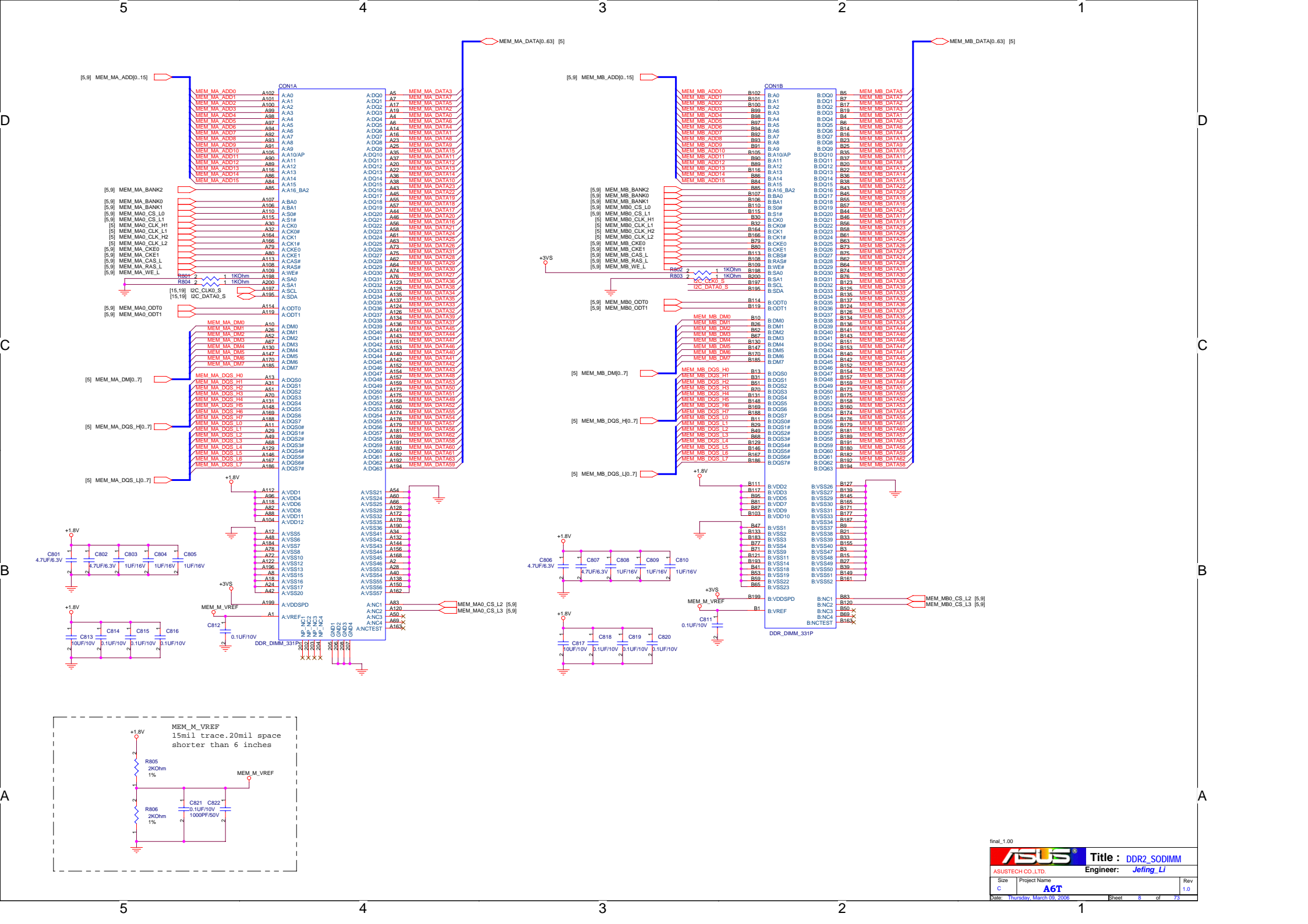


the cap close to cpu less than 1200mil
max neckdown to & from caps is 500mil

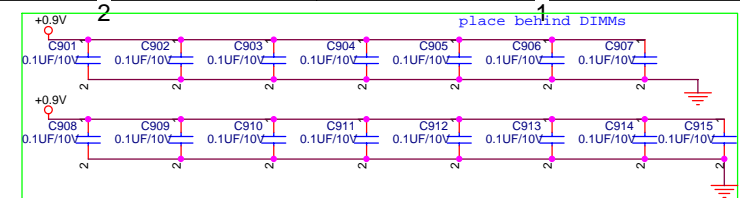
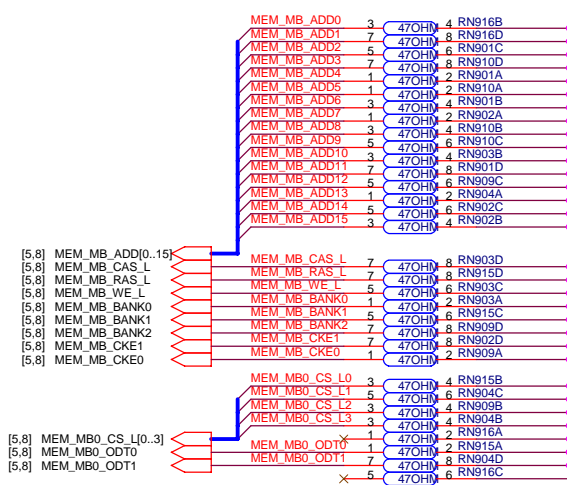
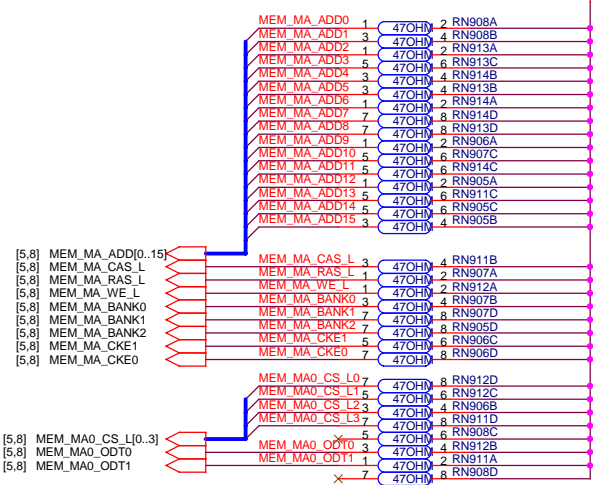




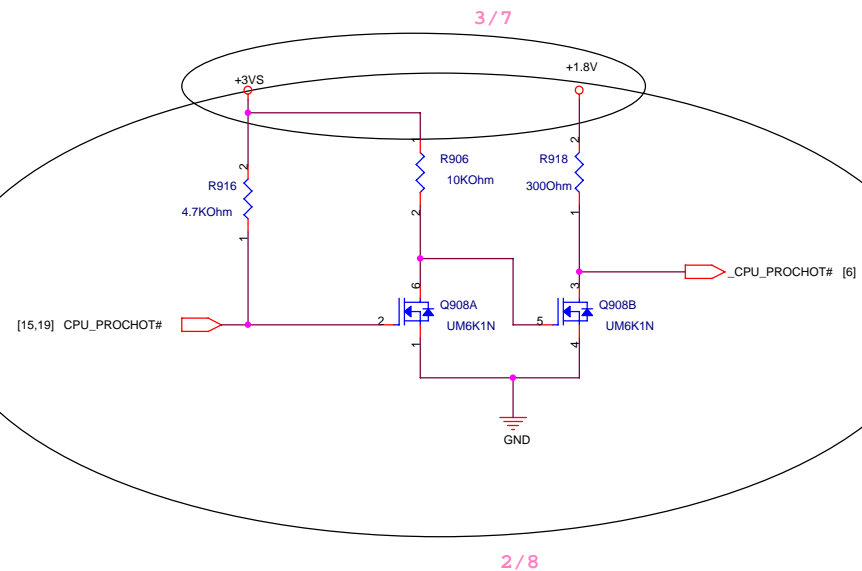
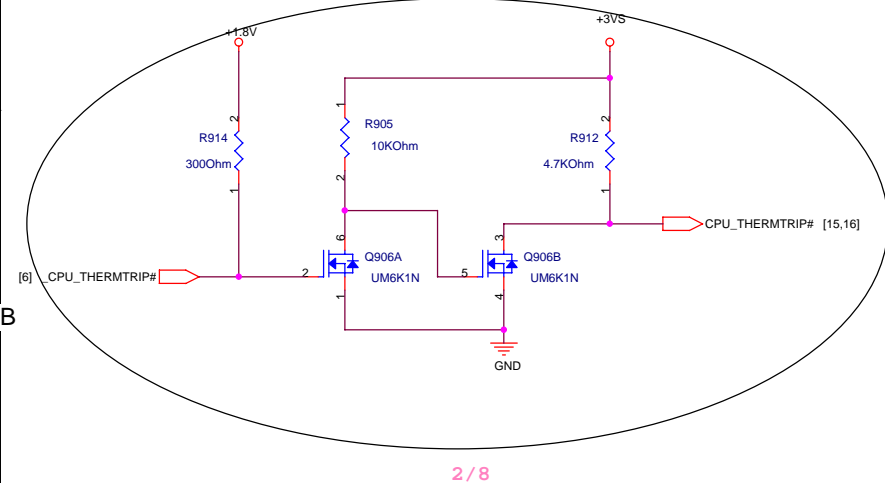


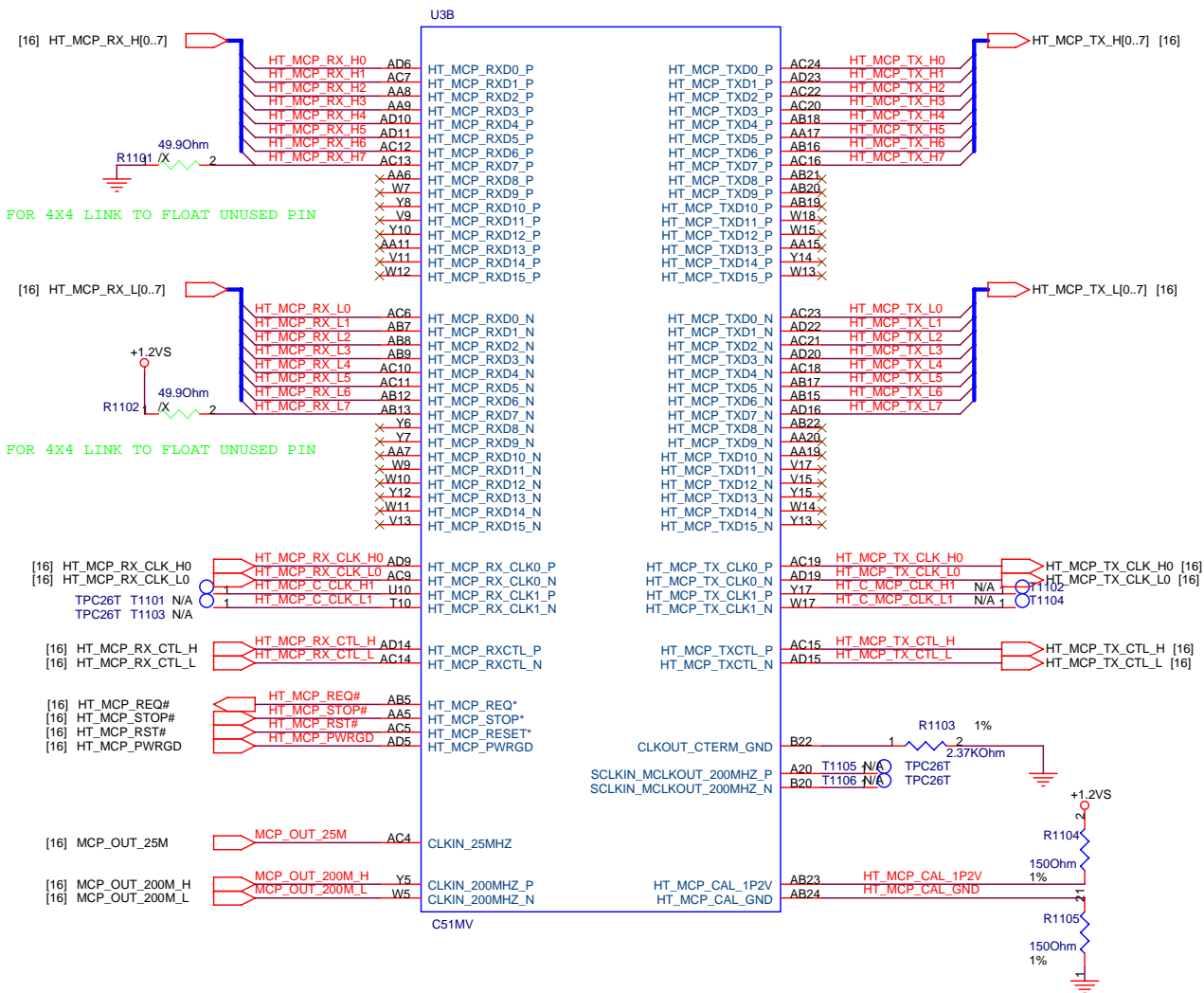


DDR2 TERMINATION

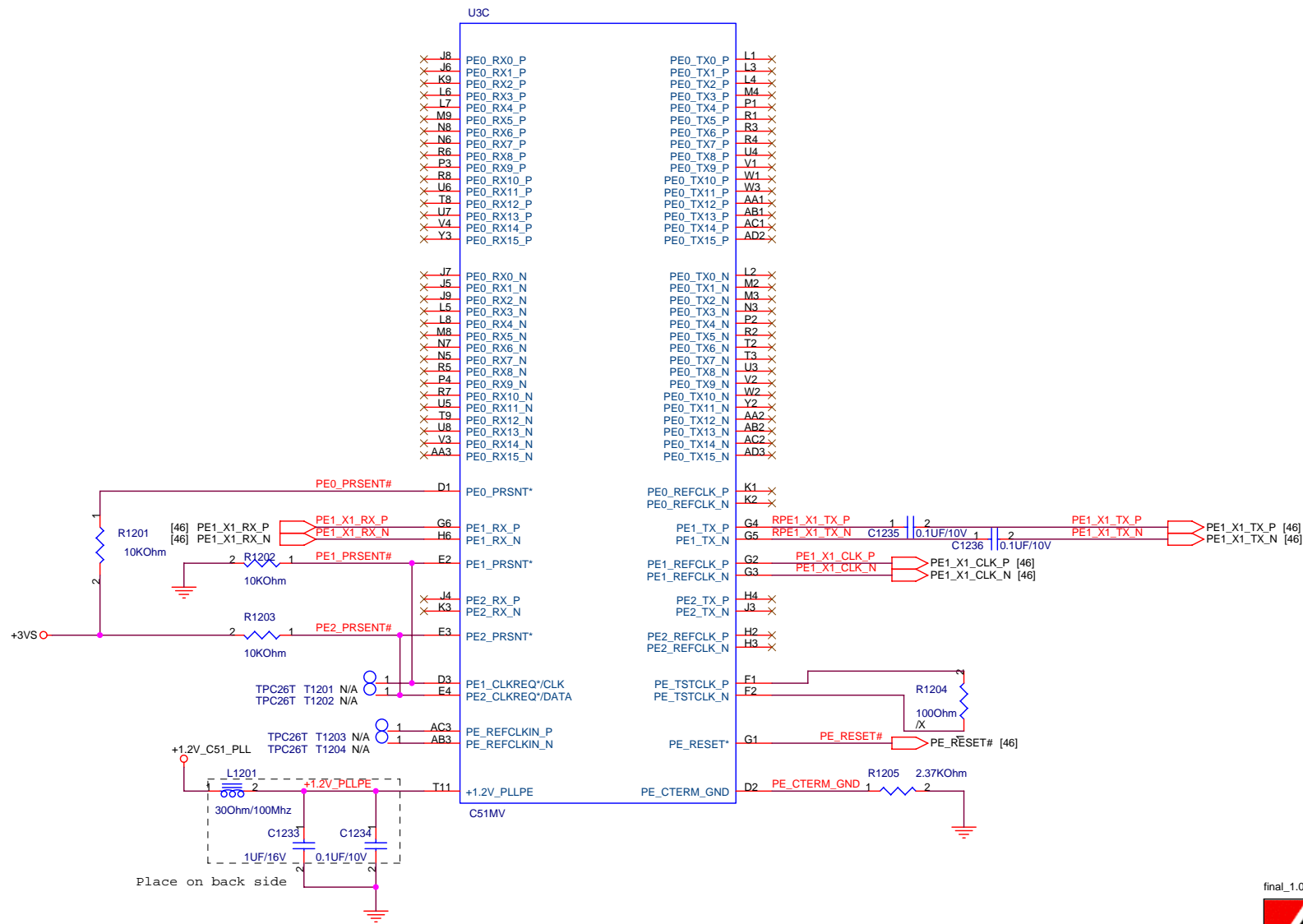


LAYOUT : COULD BE SWAP





final_1.00



final_1.00

ASUS		Title : C51_PCIE	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size B	Project Name A6M		Rev 1.0
Date: Thursday, March 09, 2006	Sheet 12 of 73		

Fan Speed Control

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

KBC will issue a
analog (a voltage
level) signal.

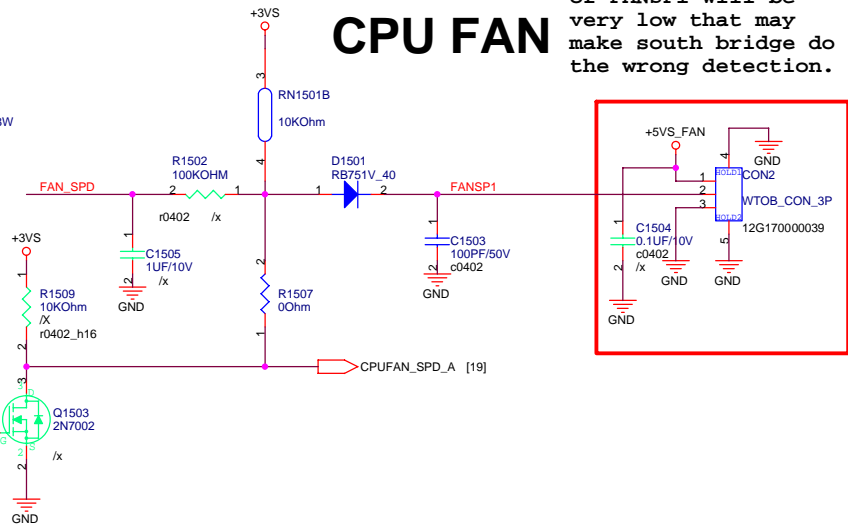
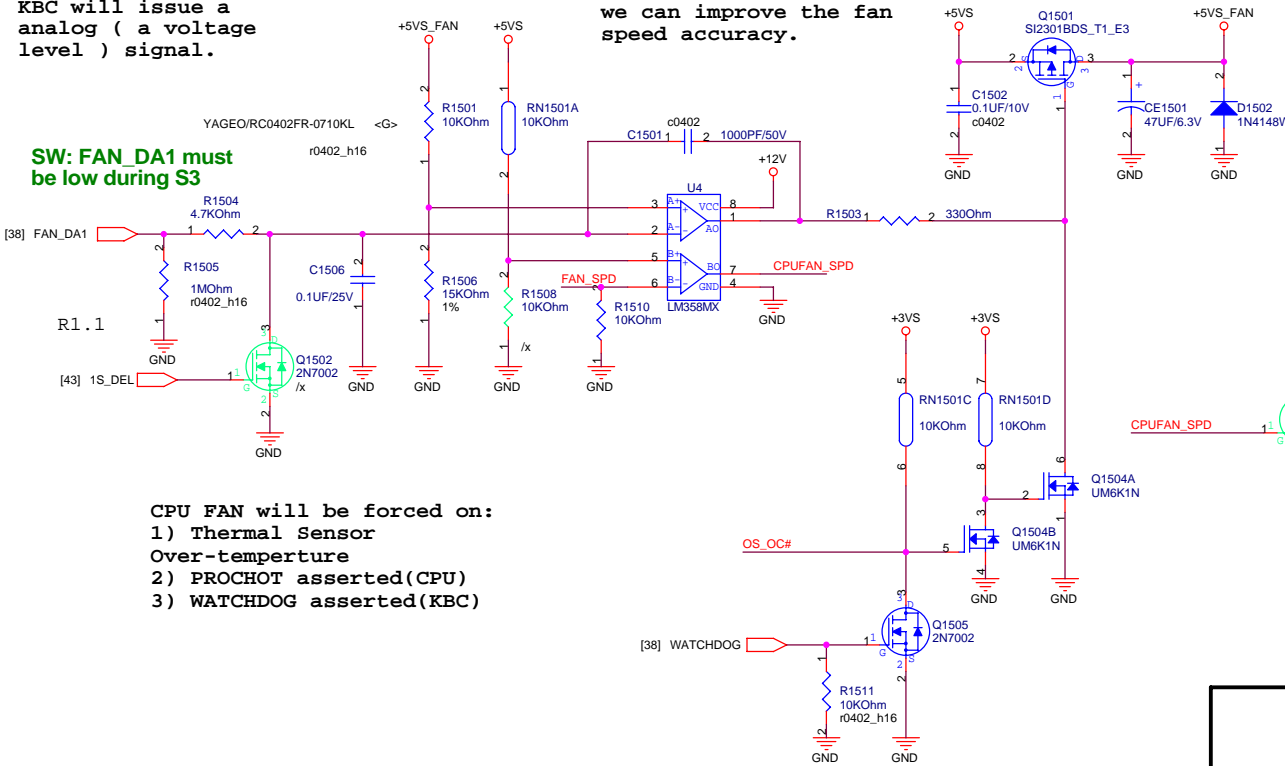
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

CPU FAN

SW: FAN_DA1 must be low during S3

CPU FAN will be forced on:

- 1) Thermal Sensor Over-temperature
- 2) PROCHOT asserted(CPU)
- 3) WATCHDOG asserted(KBC)

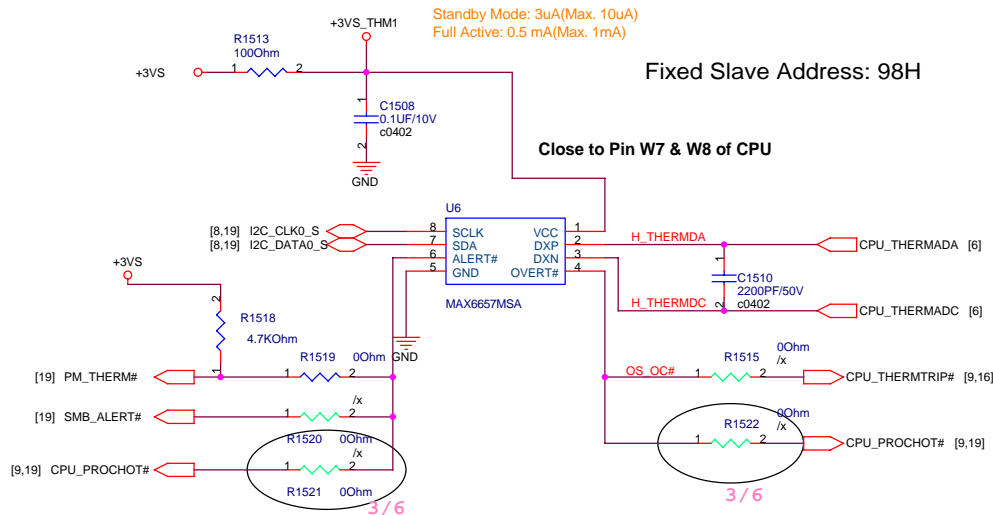


CPU THERM SENSOR

Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

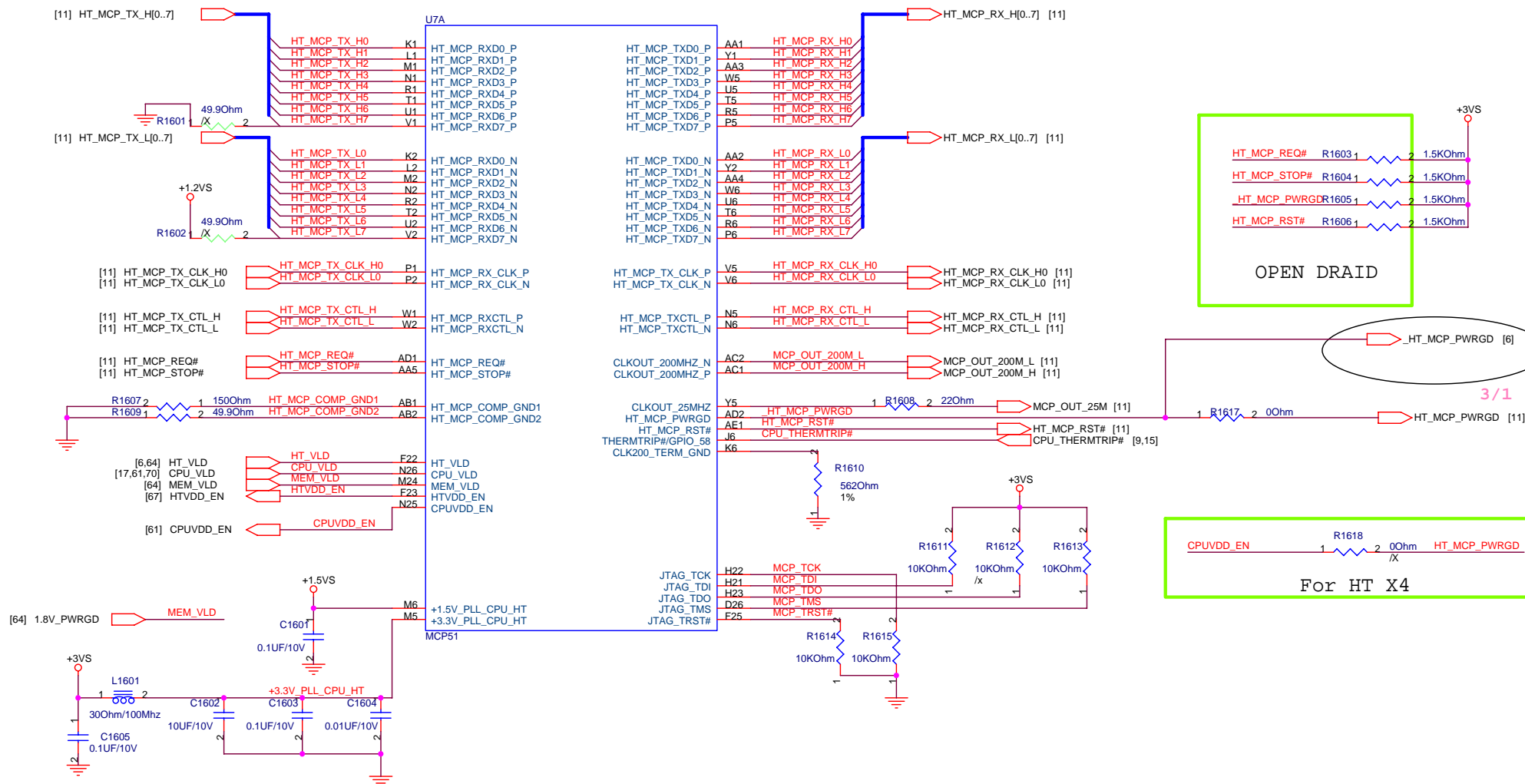
Fixed Slave Address: 98H

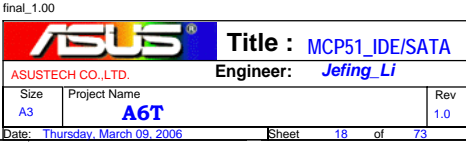
Close to Pin W7 & W8 of CPU

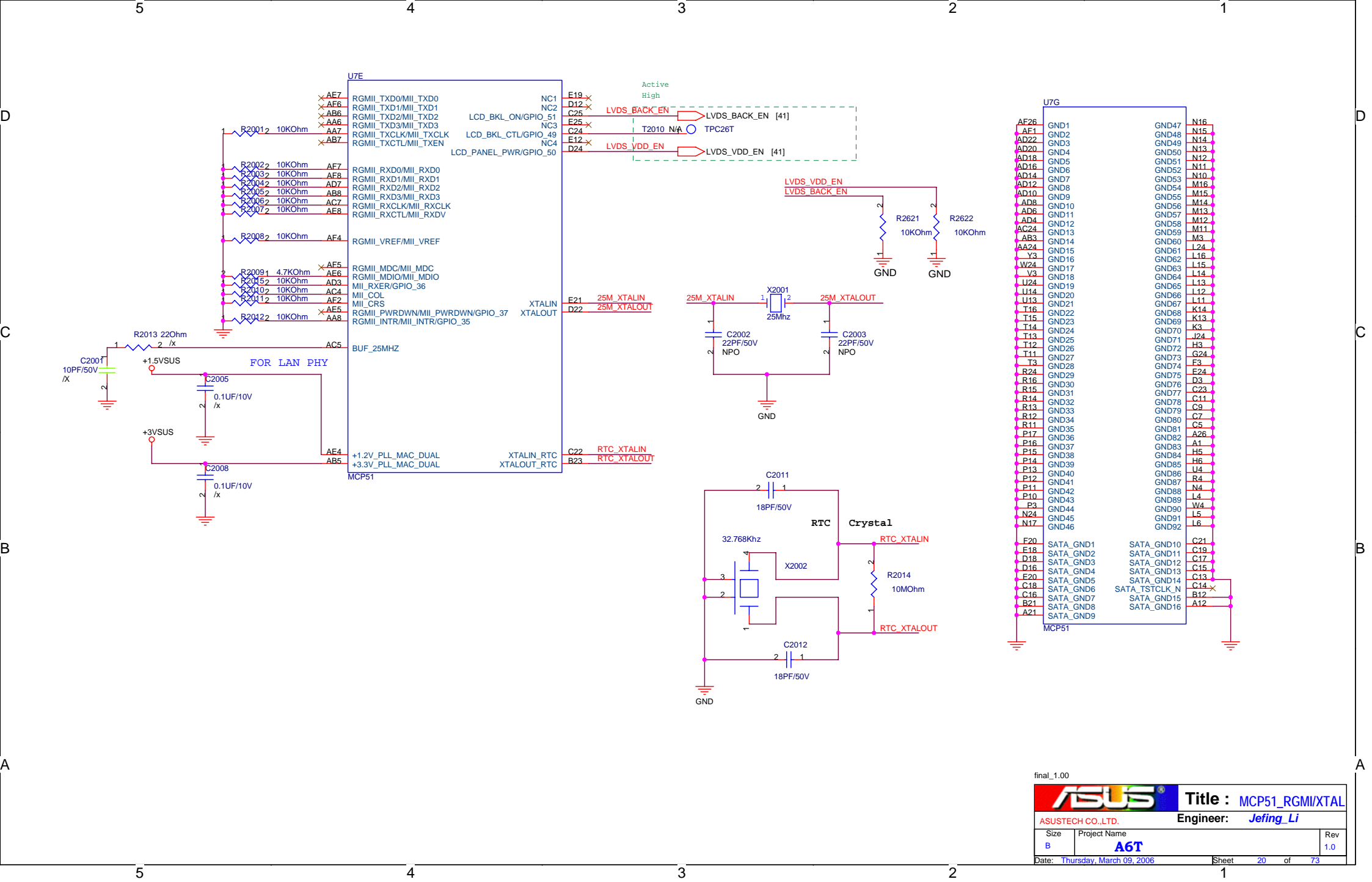


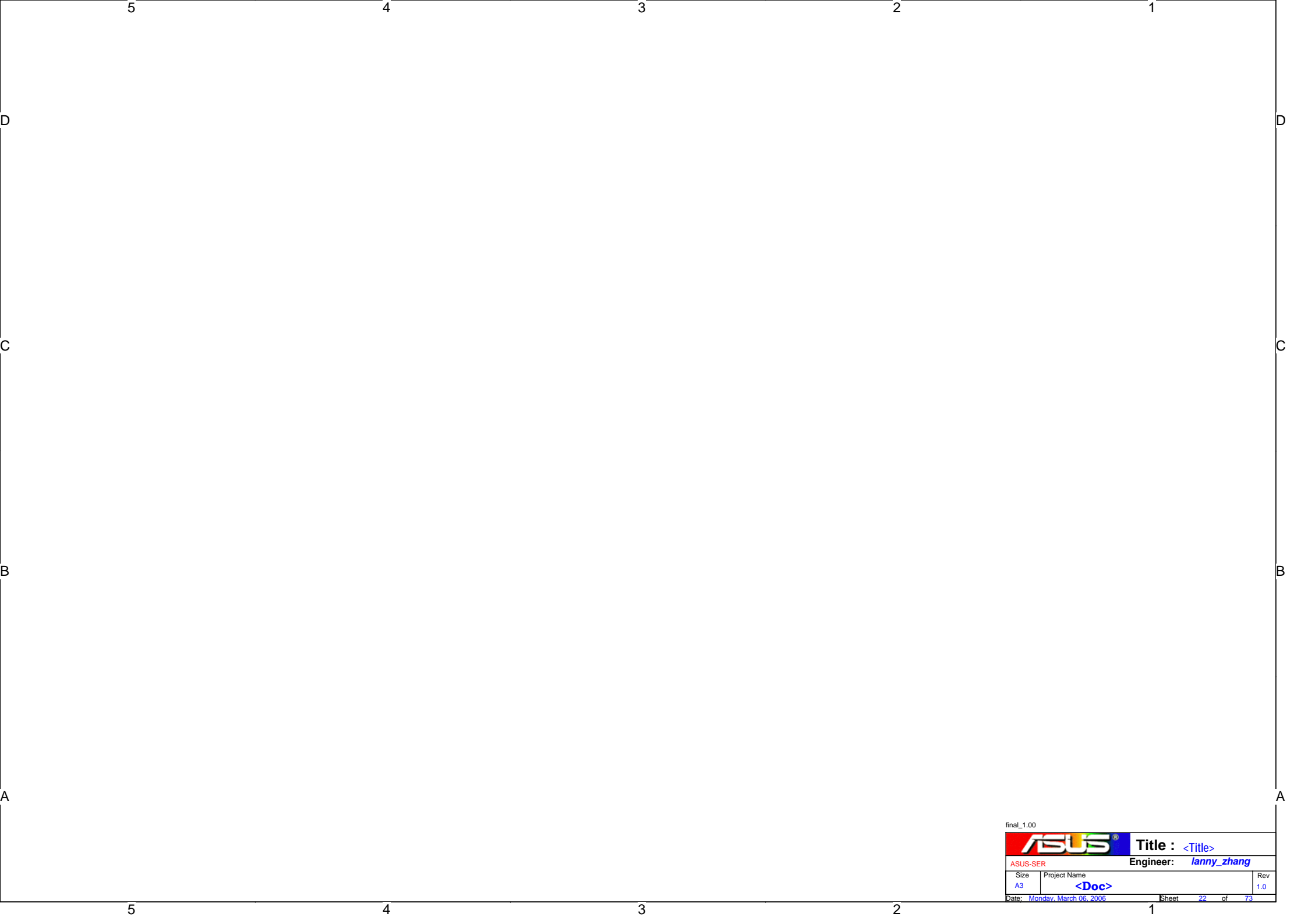
final_1.00

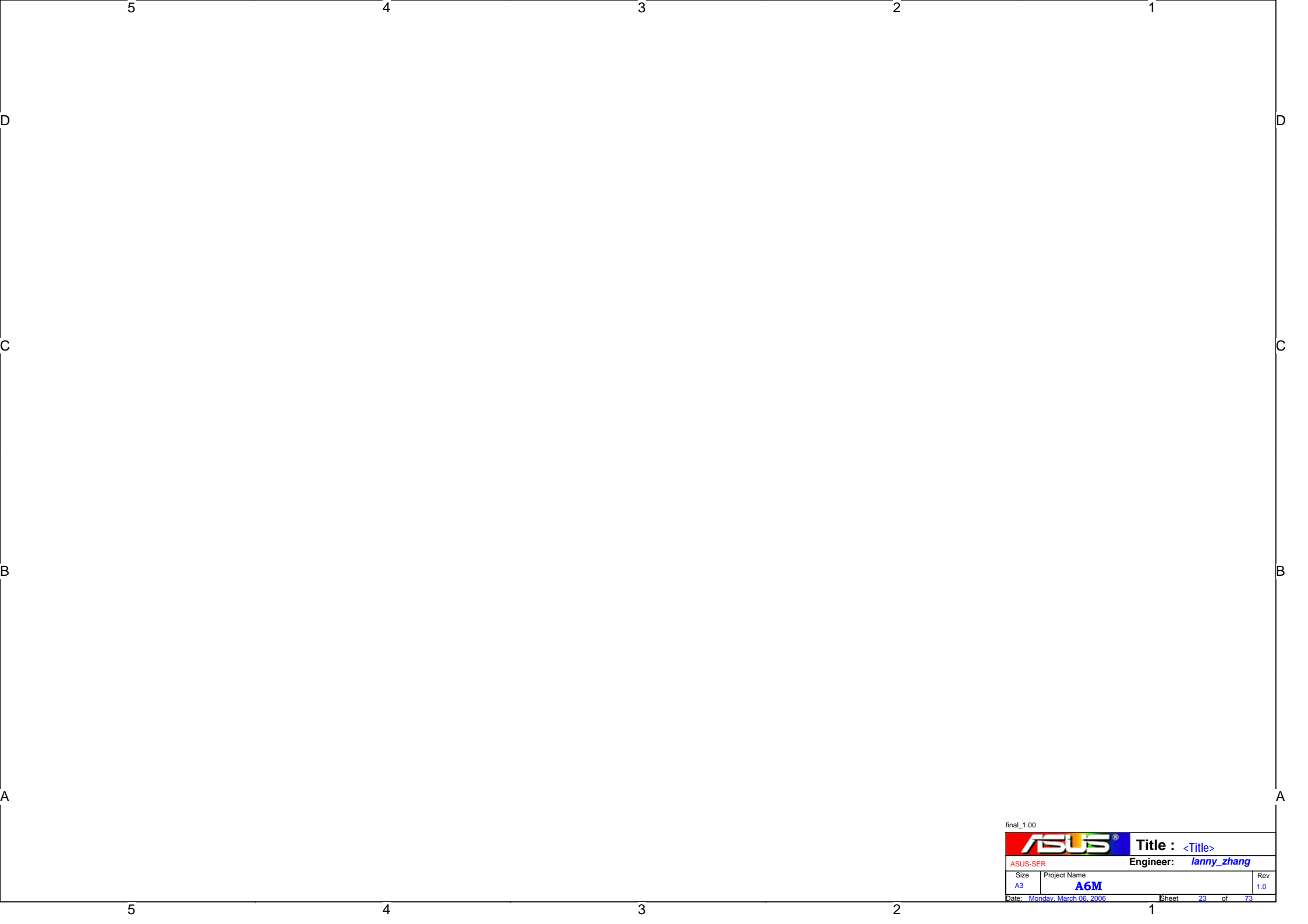


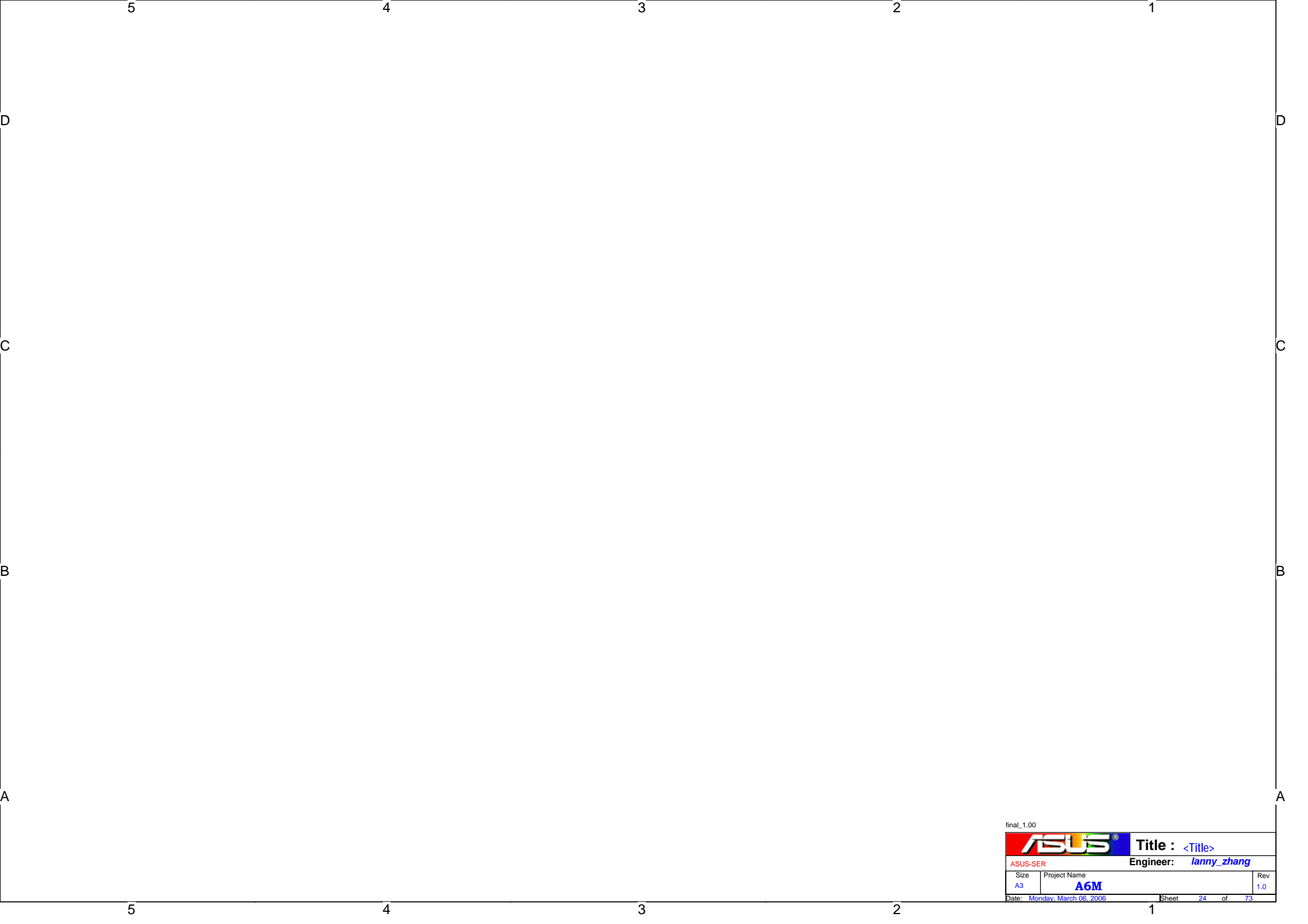


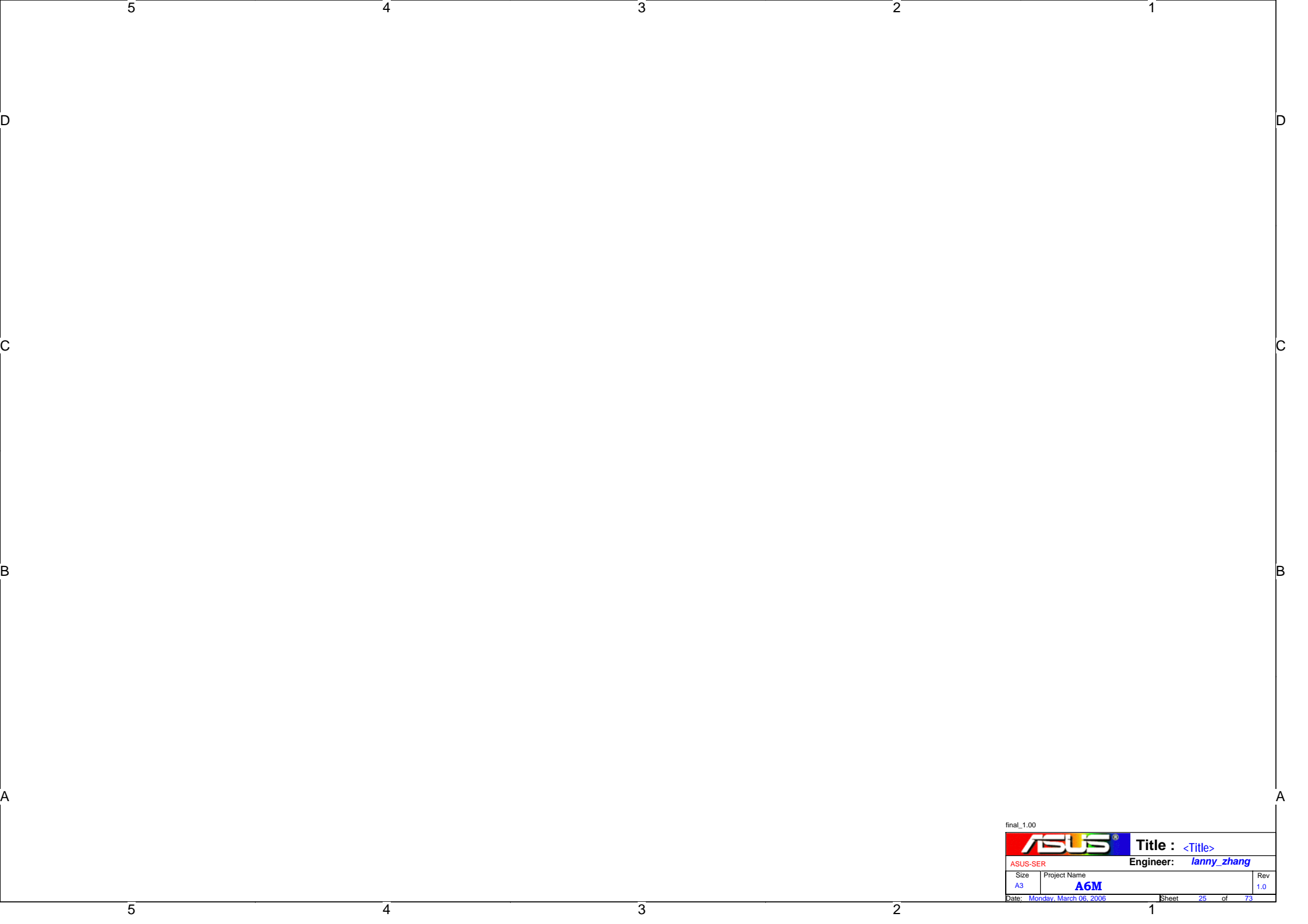


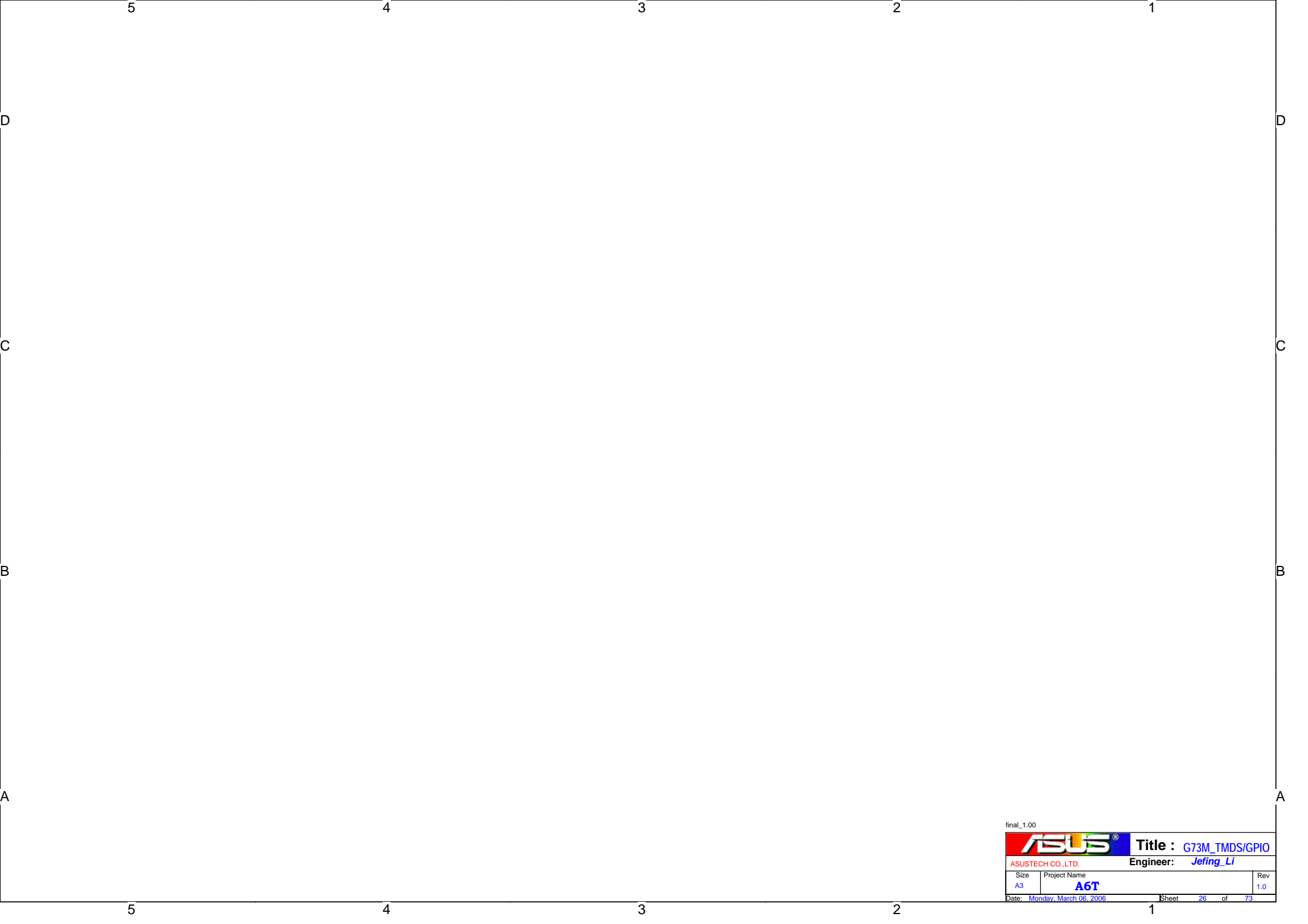


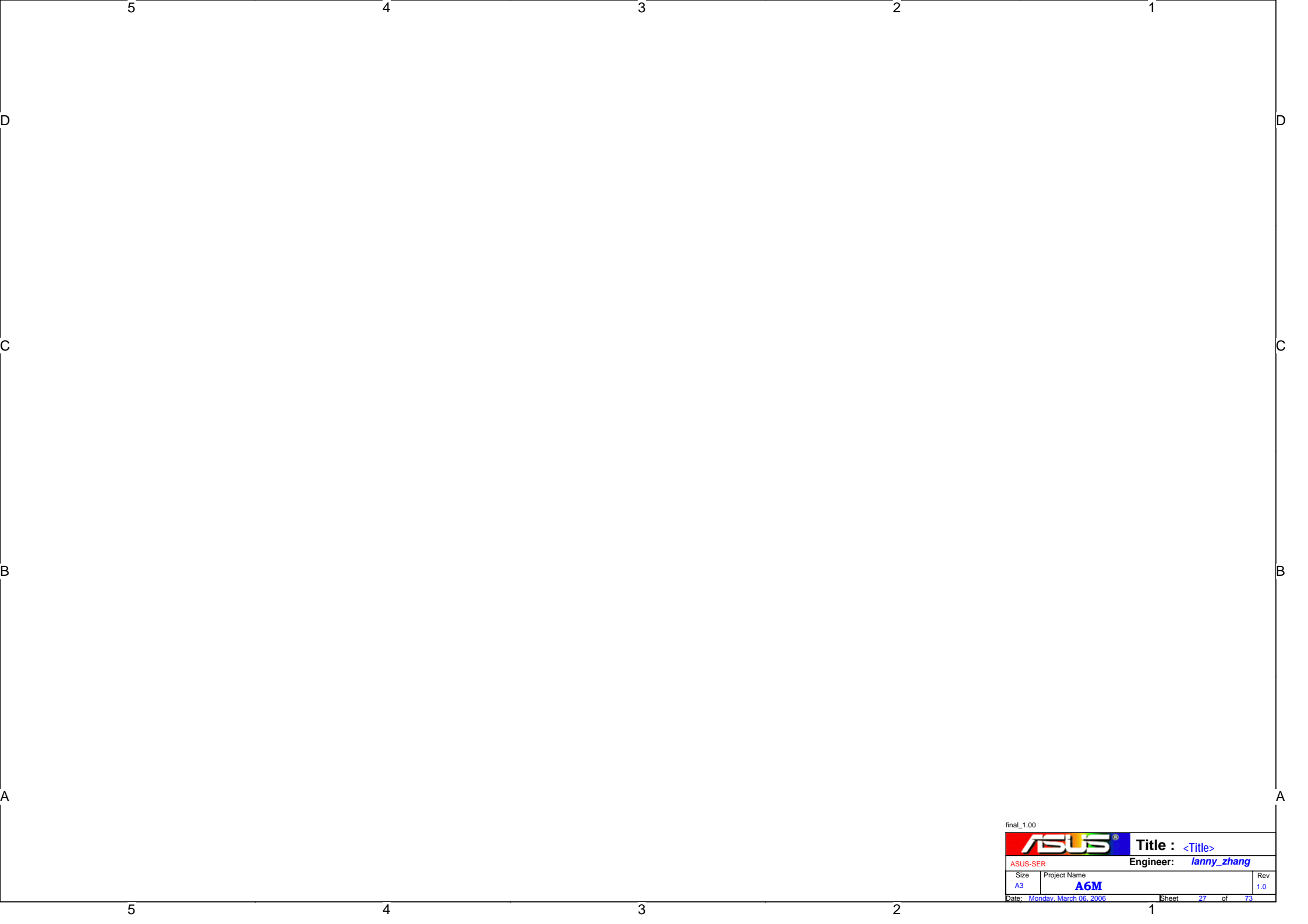


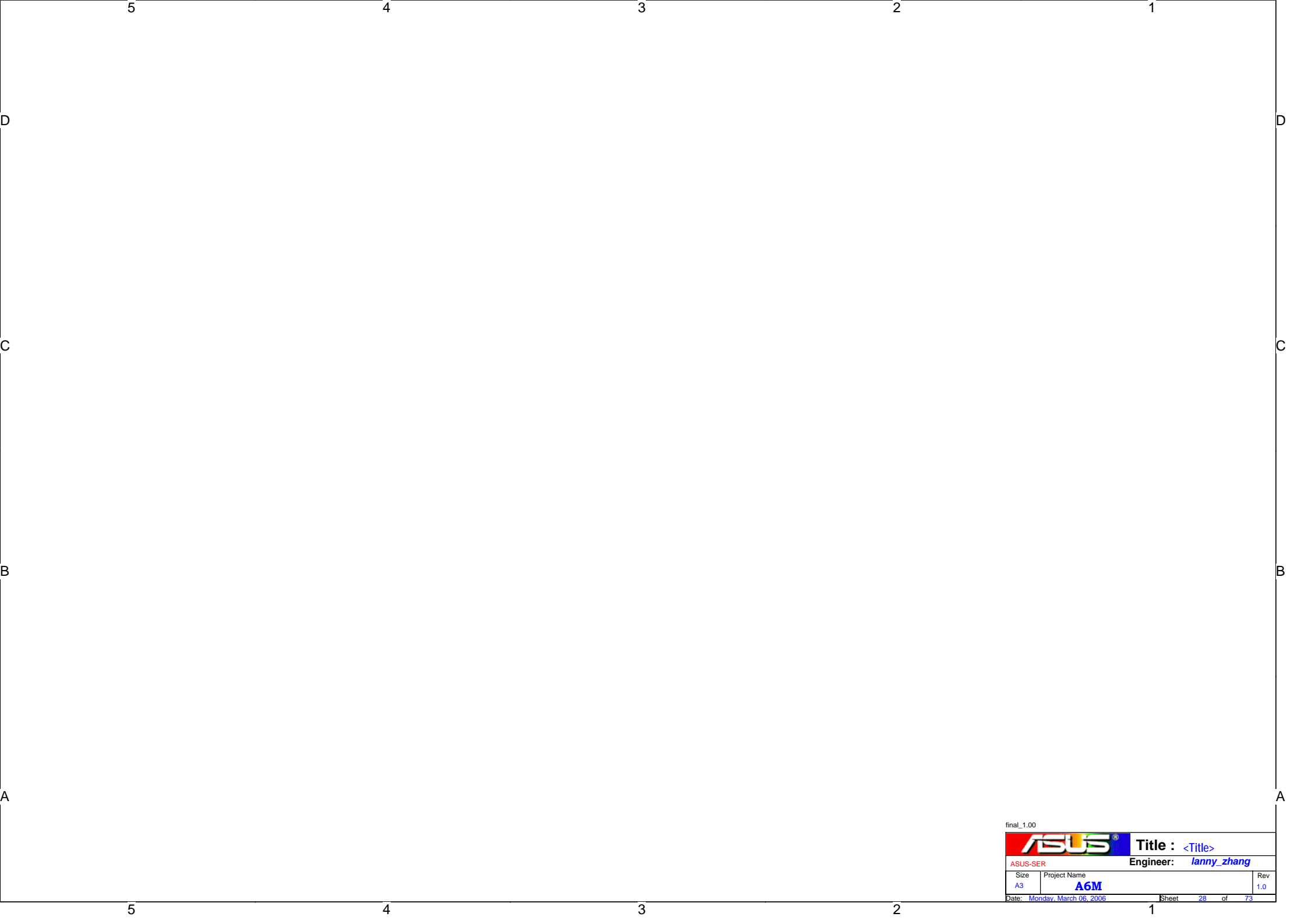


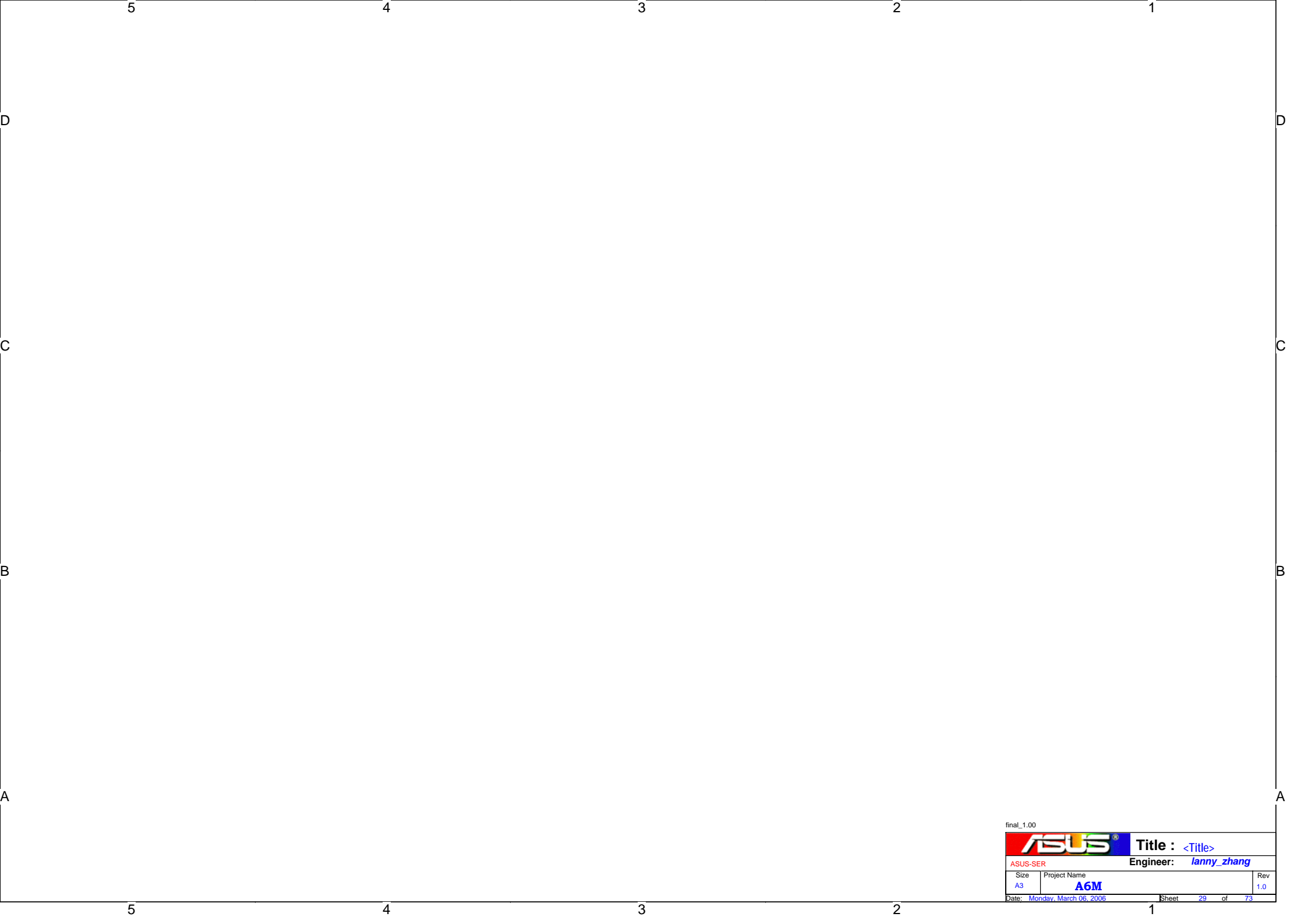


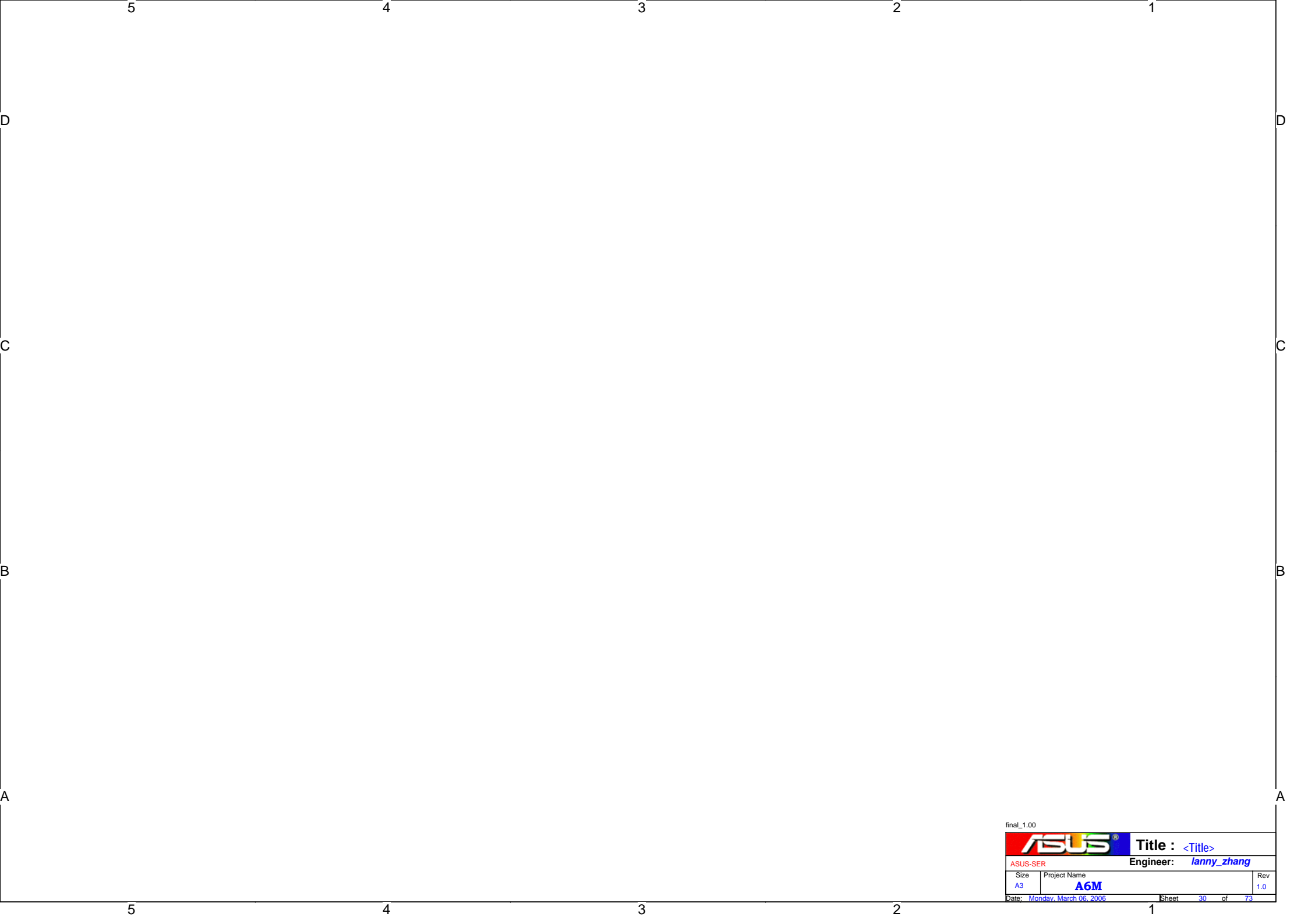


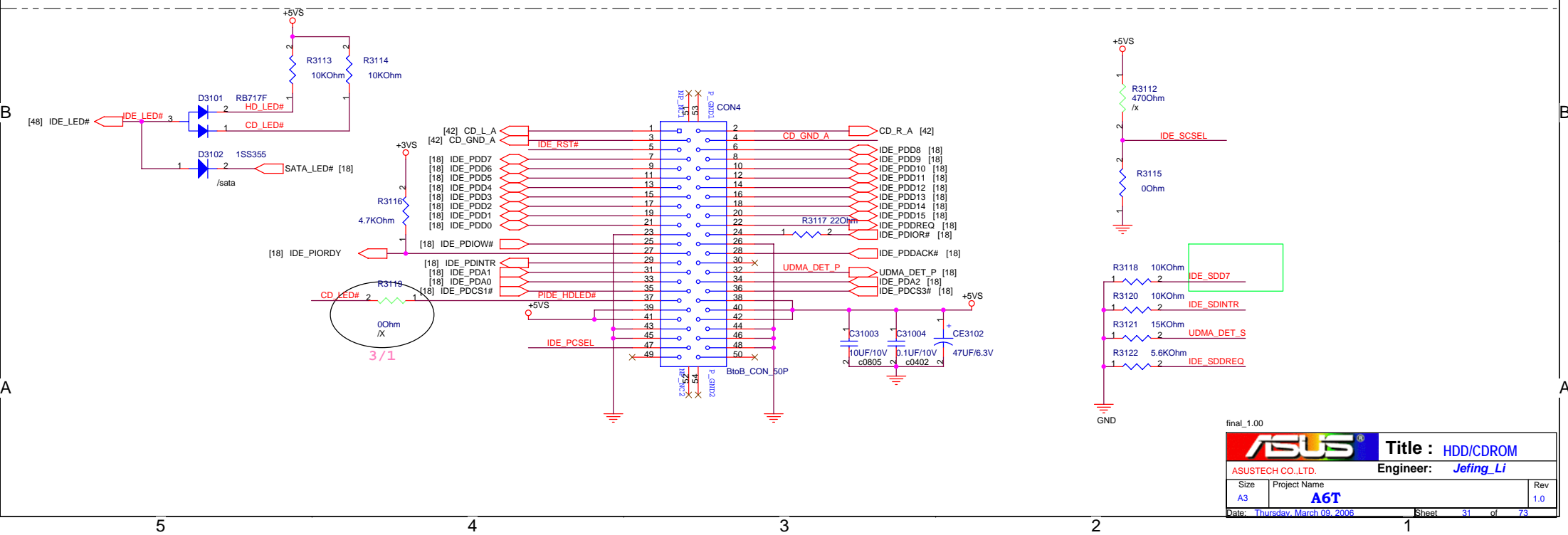
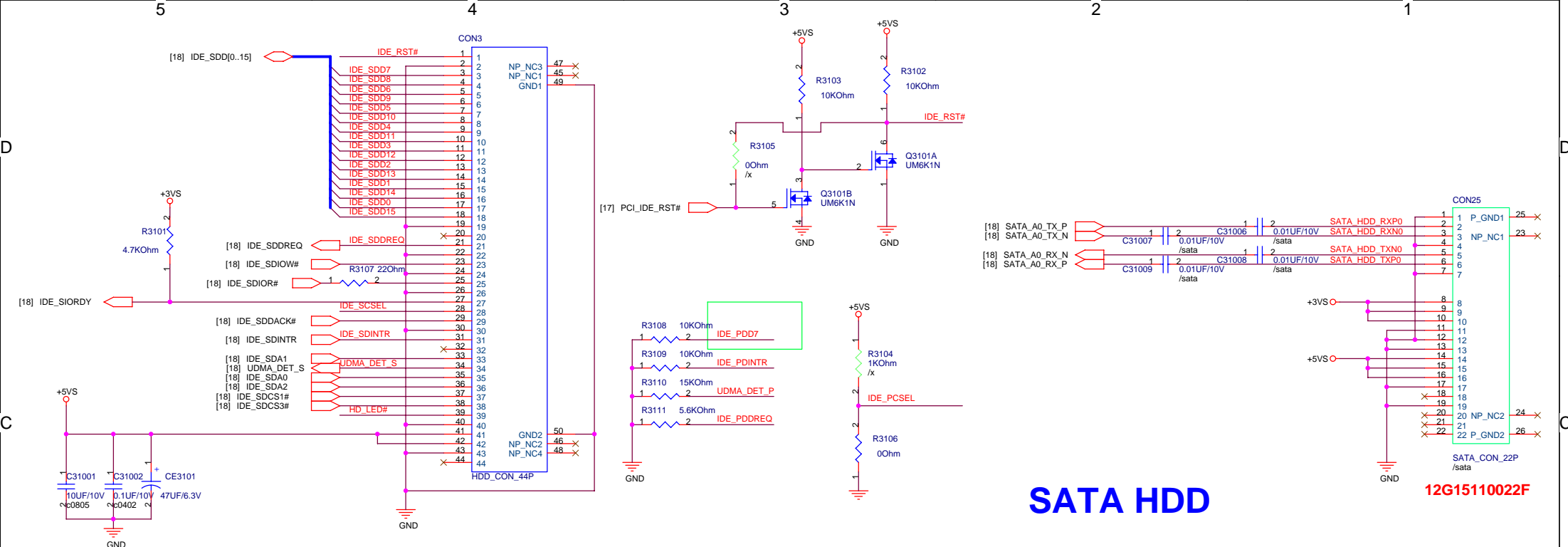


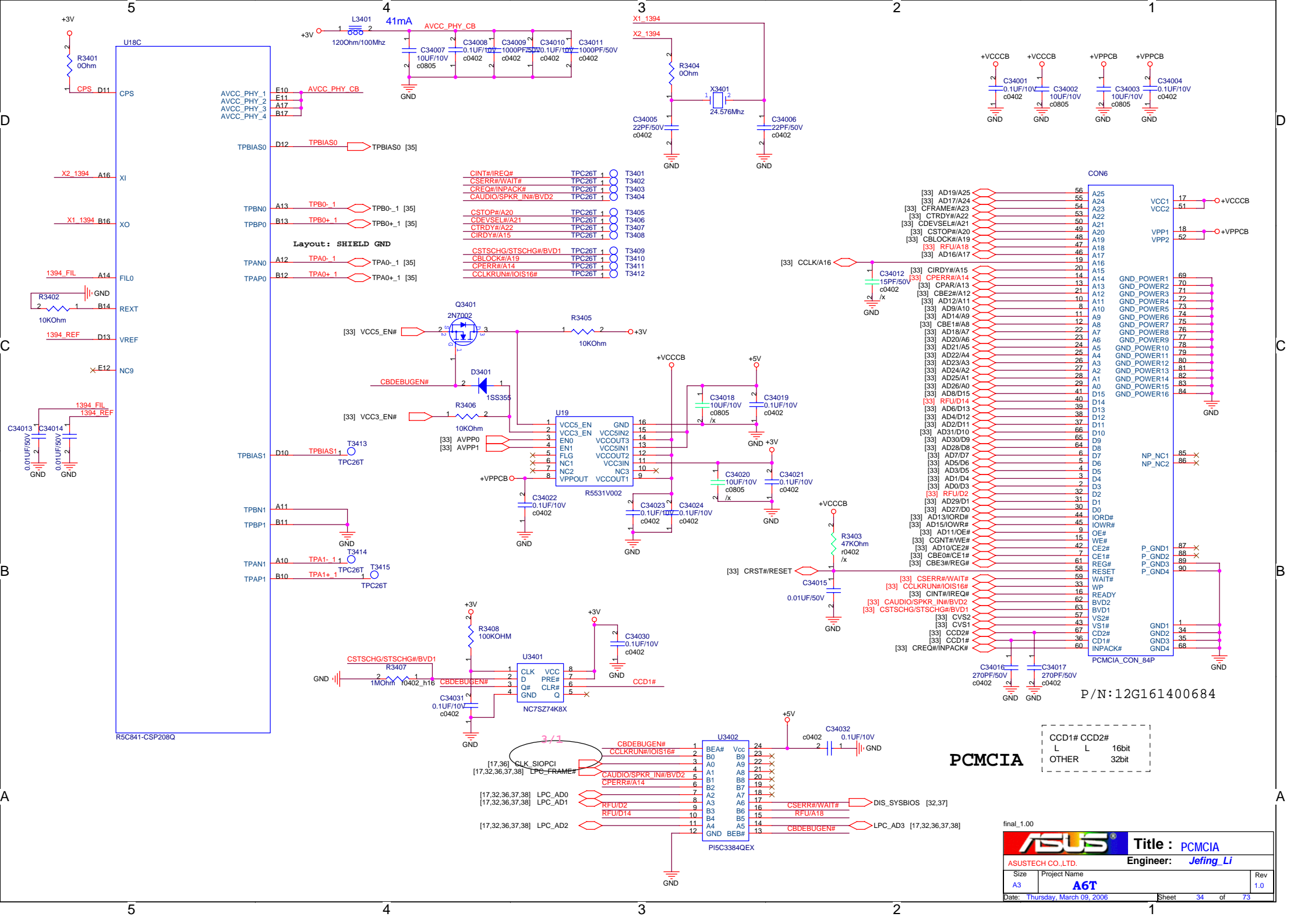


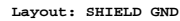
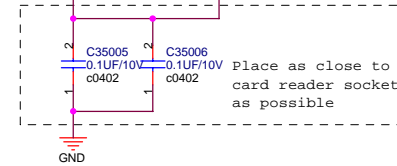
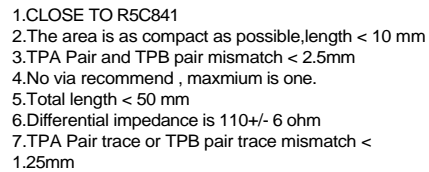
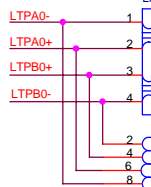




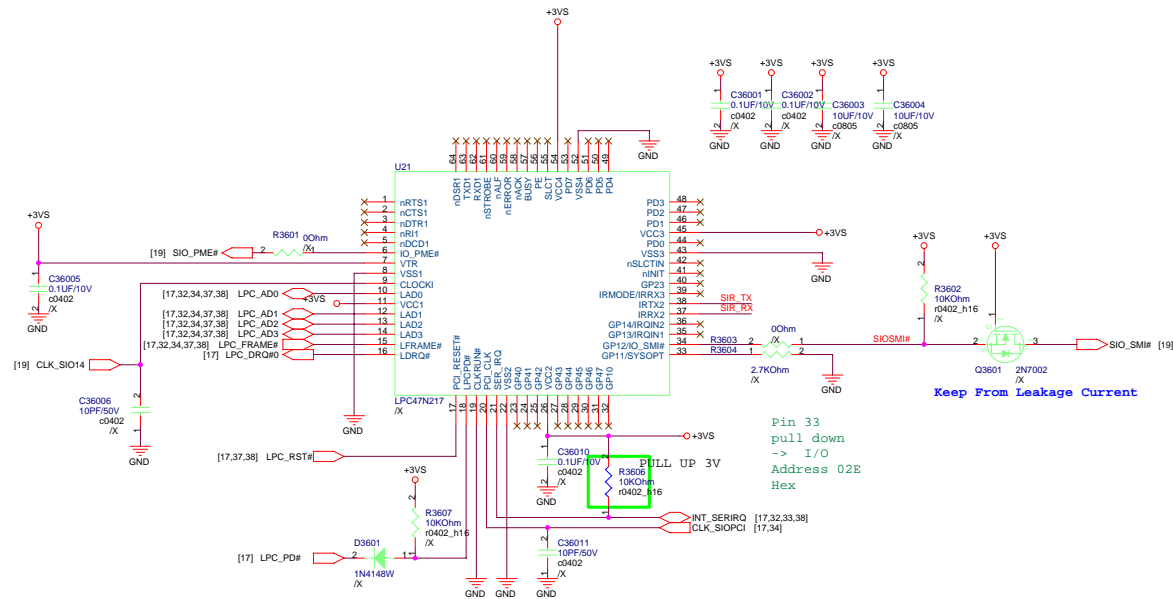




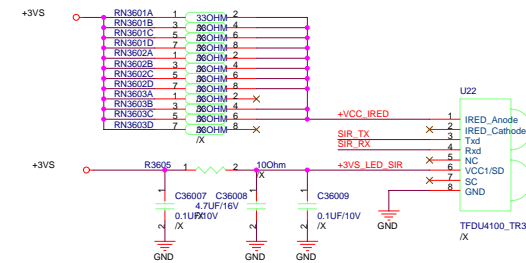




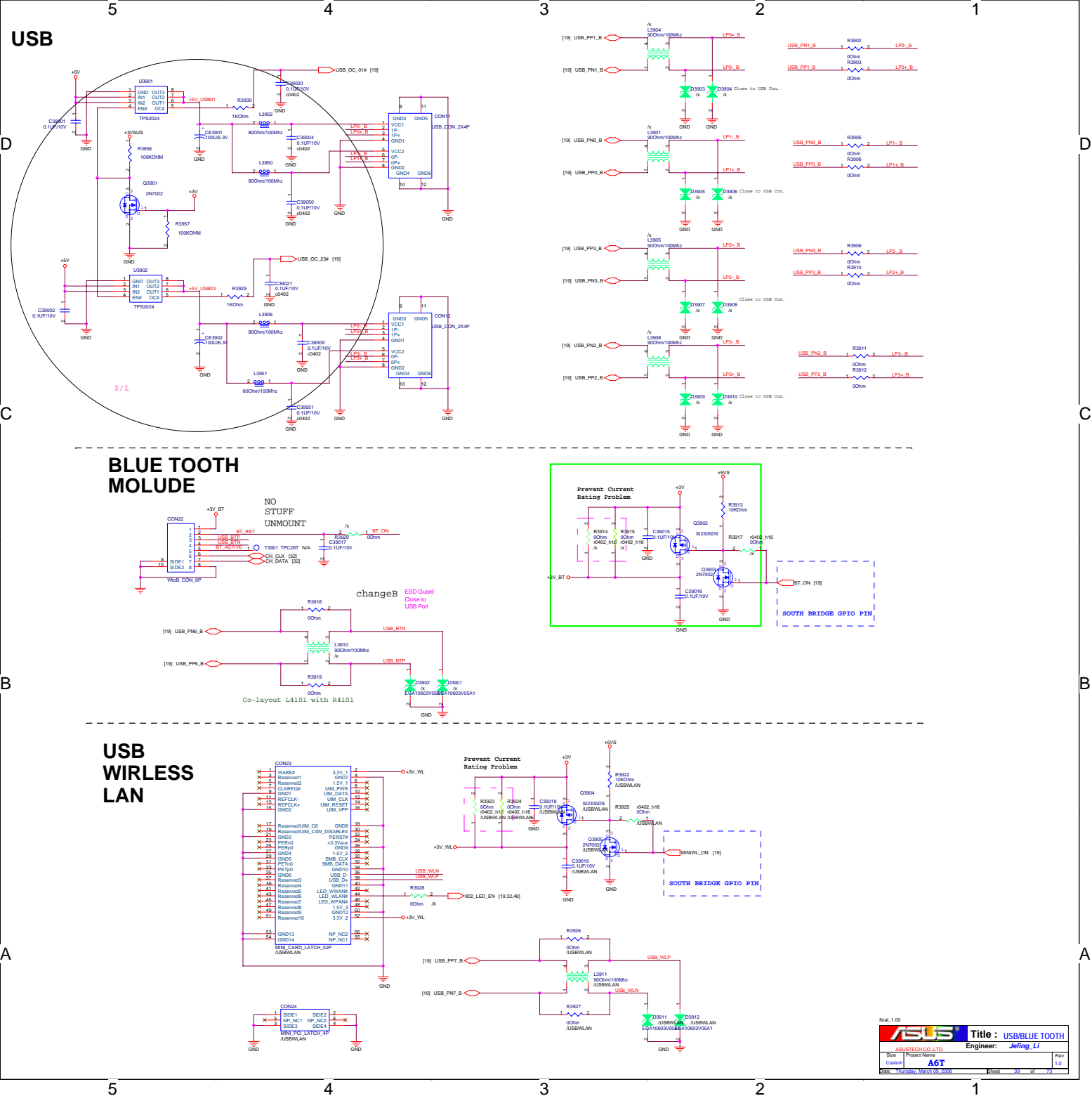
Super I/O

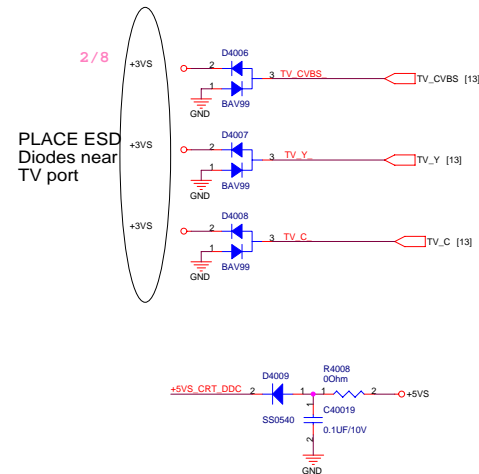
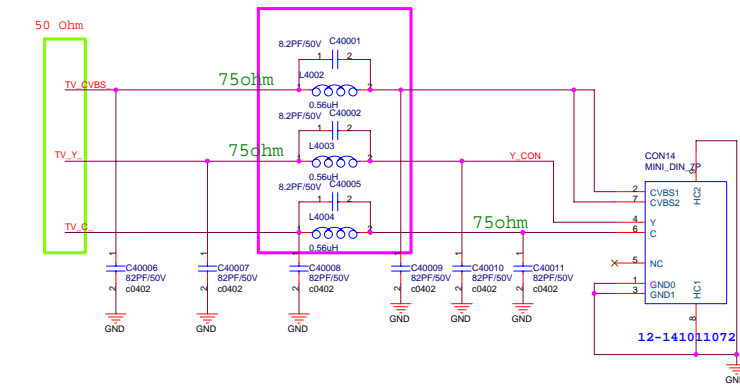
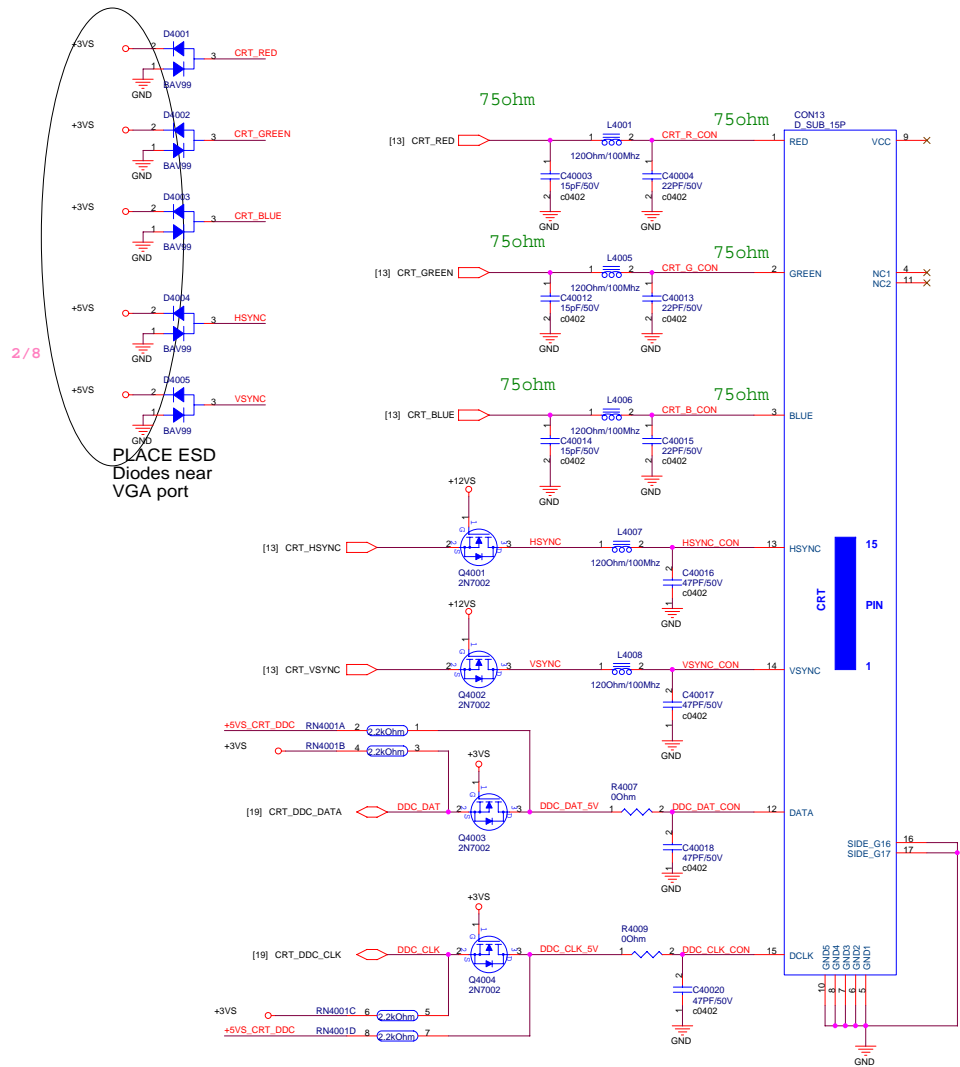


SIR



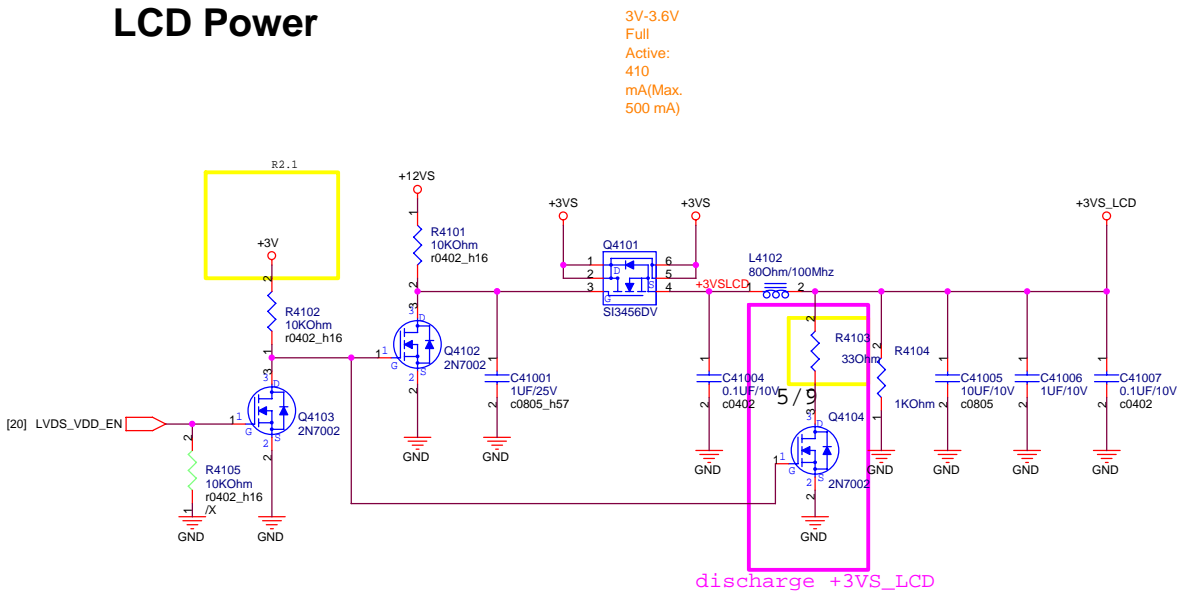
A



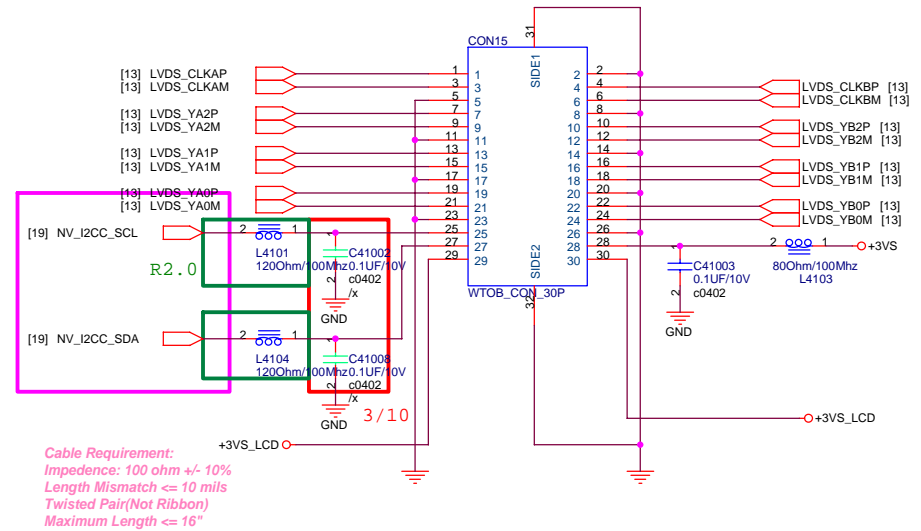


final_1.00

LCD Power

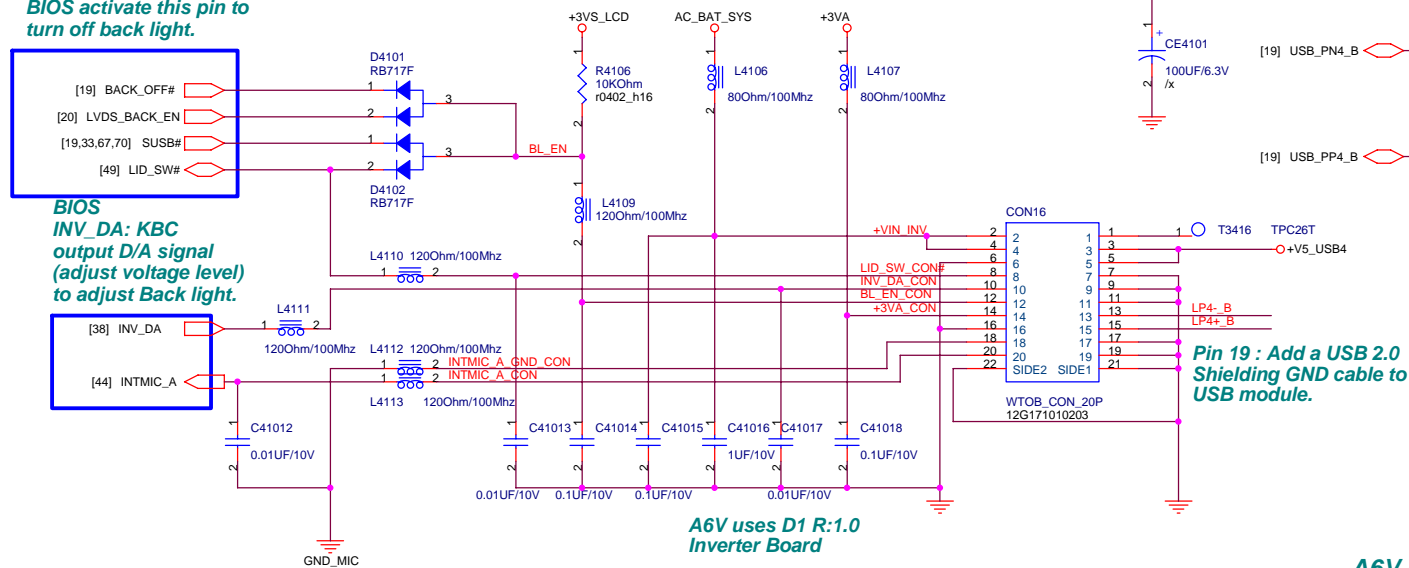


LCD LVDS Interface

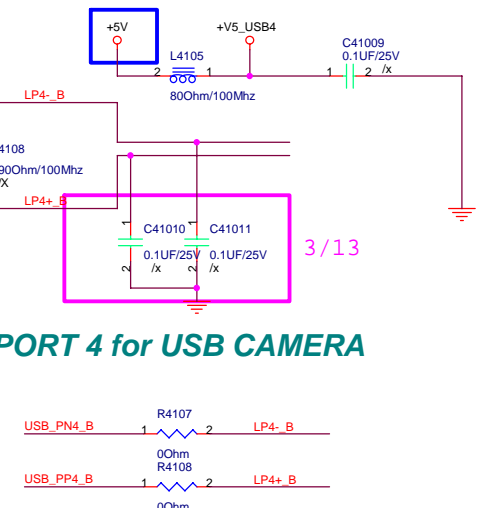


INVERTER Interface

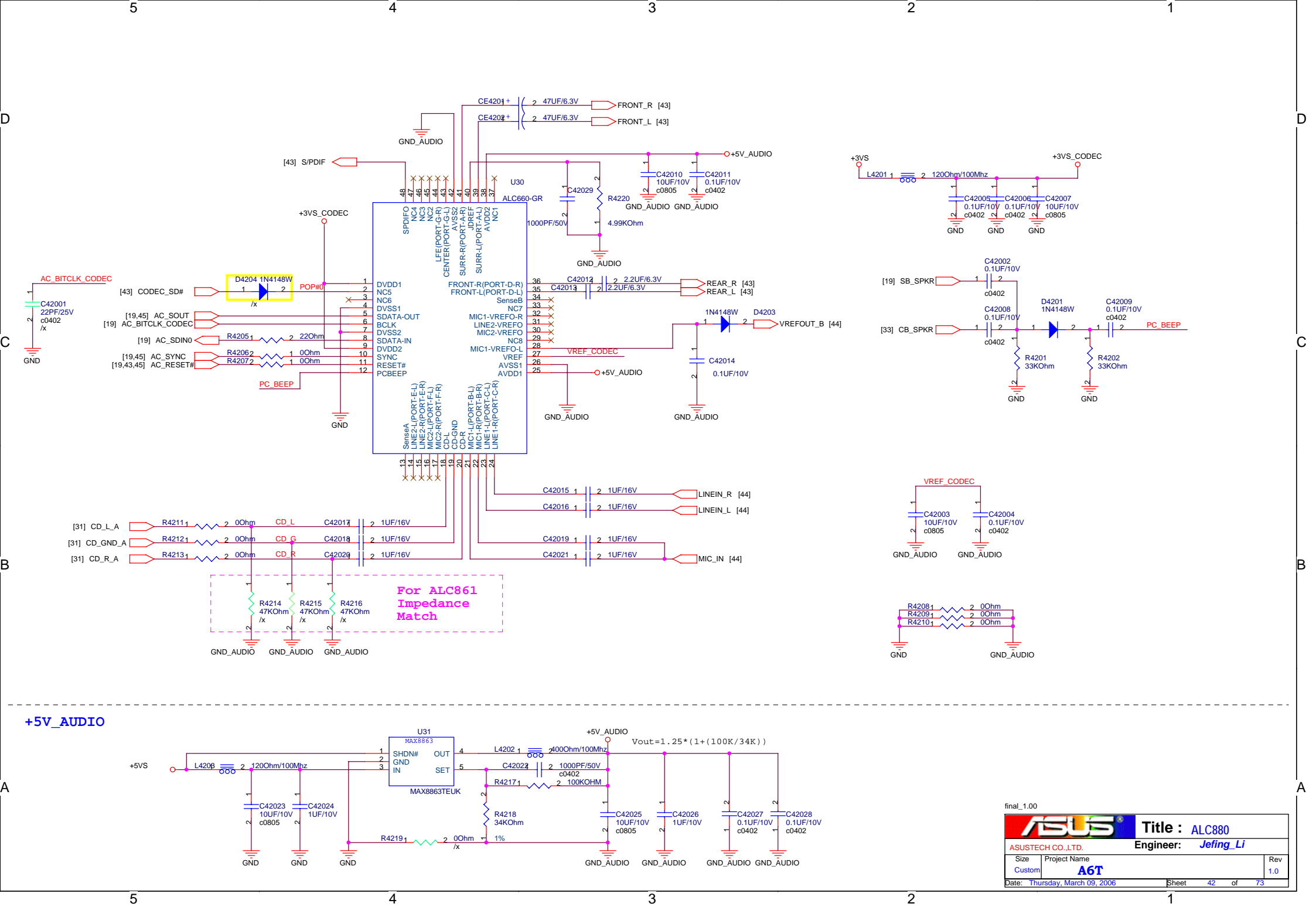
BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.



USB PORT 4 for USB CAMERA

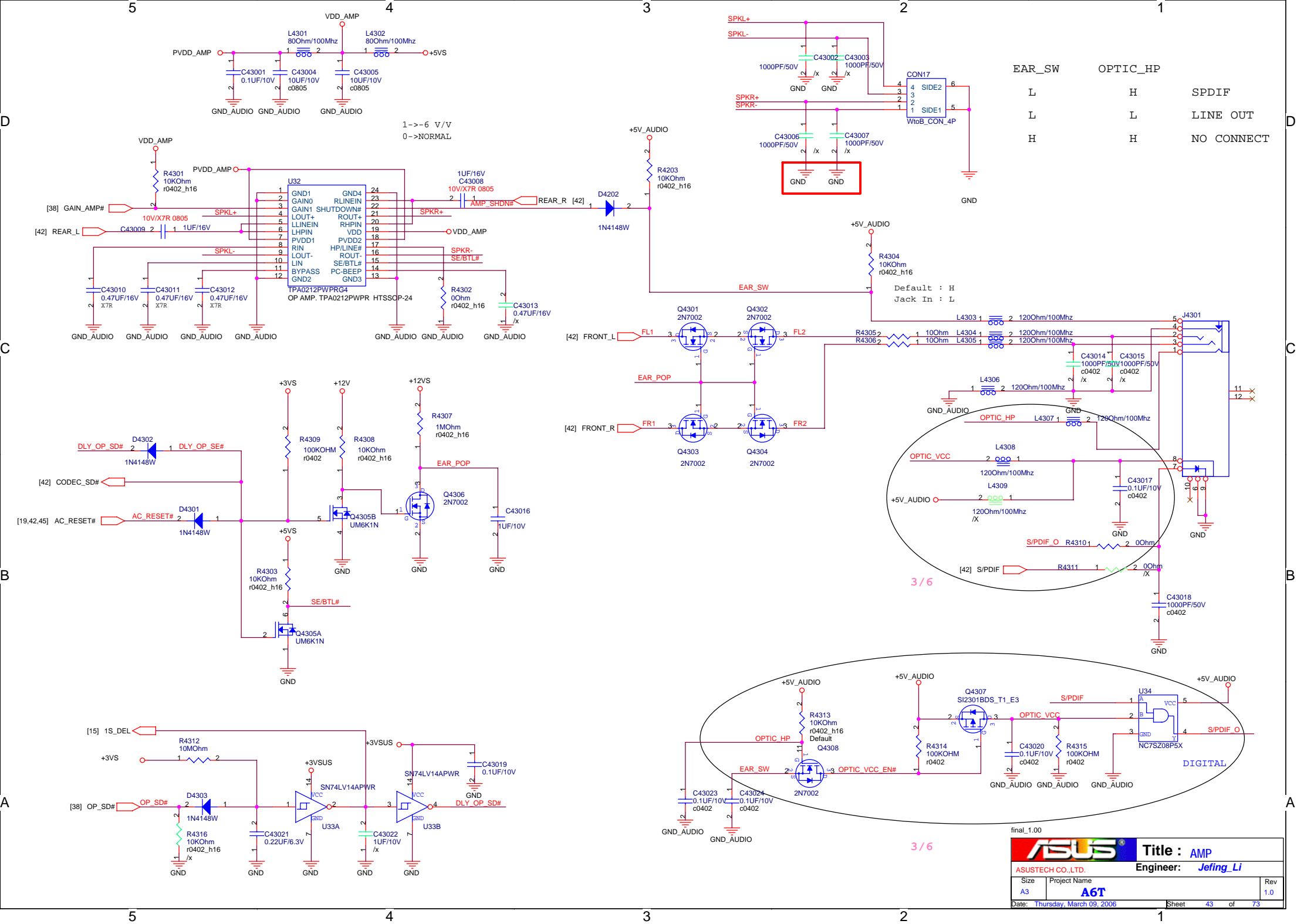


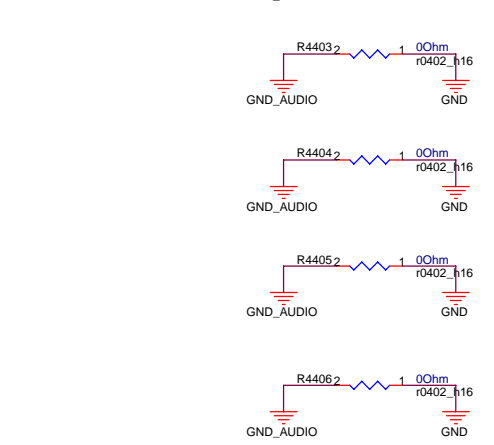
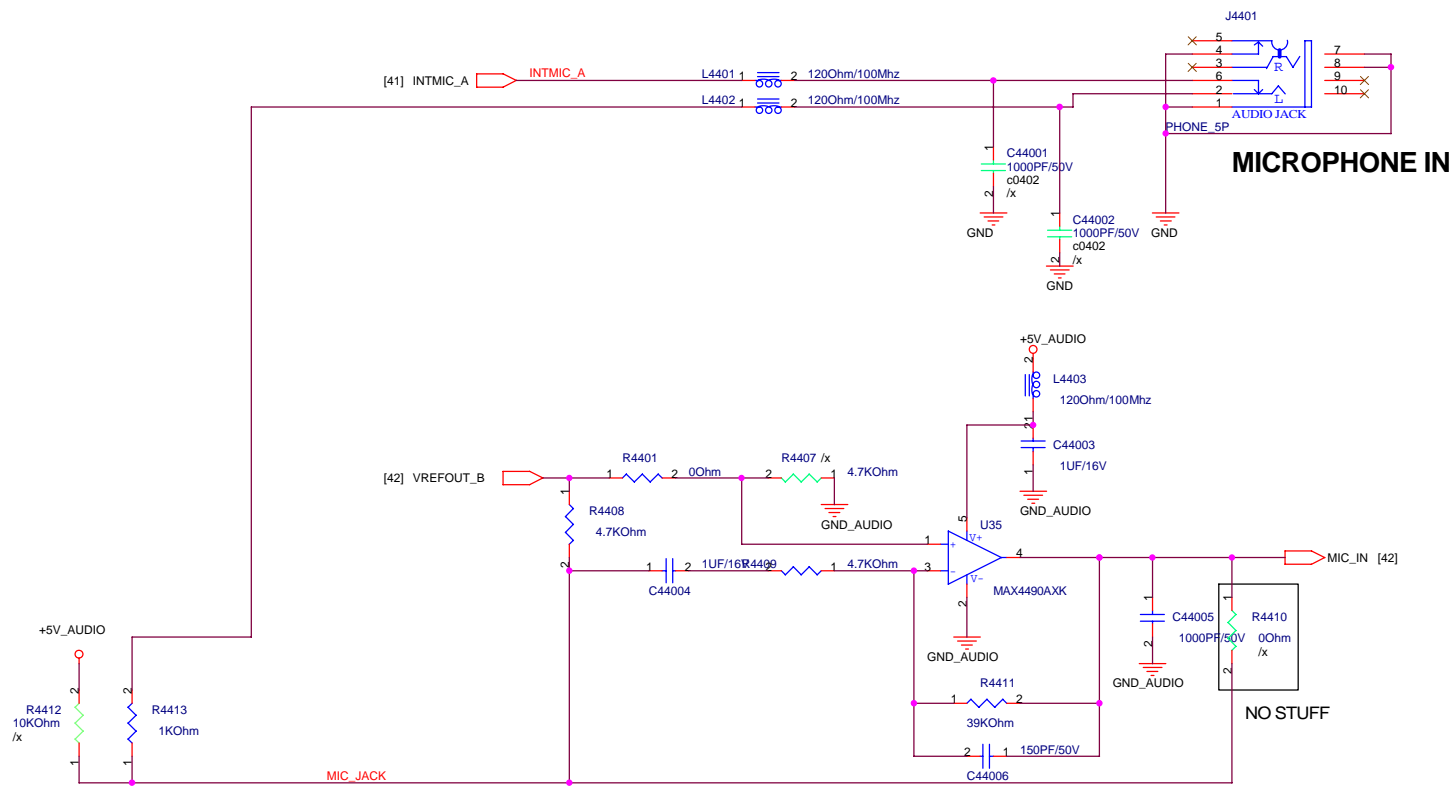
A6V doesn't support USB WLAN function! final



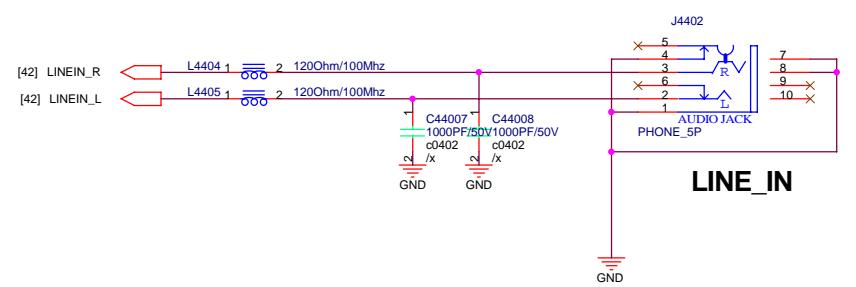
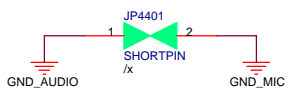
final_1.00

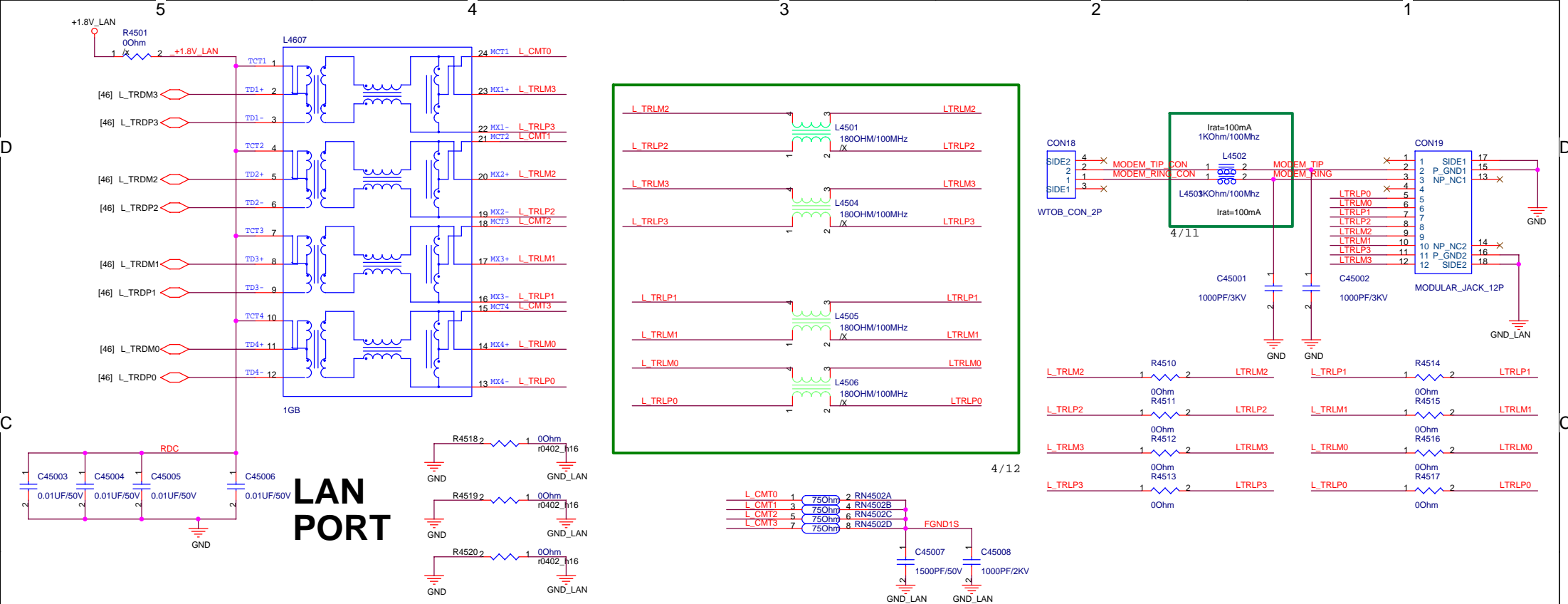
ASUS		Title : ALC880	
ASUSTECH CO., LTD.		Engineer: Jefing_Li	
Size	Project Name	Rev	
Custom	A6T	1.0	
Date: Thursday, March 09, 2006		Sheet	42 of 73



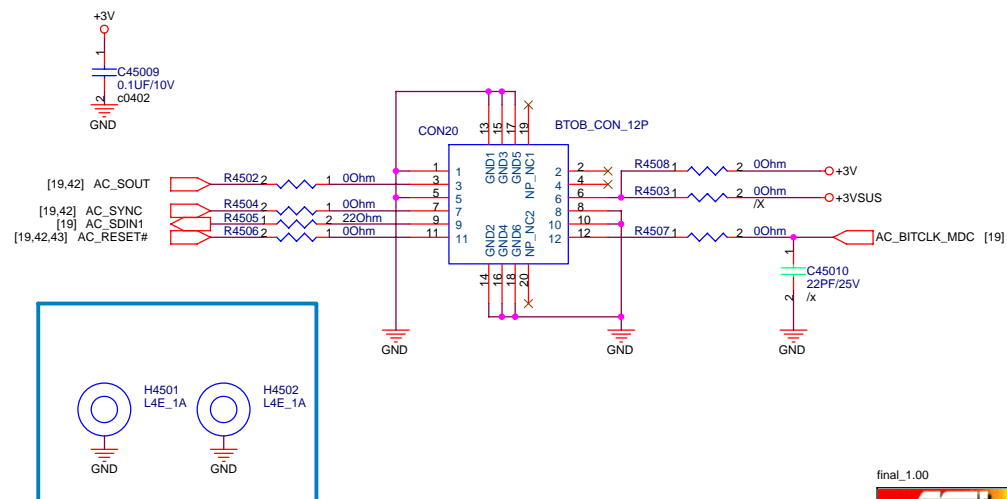


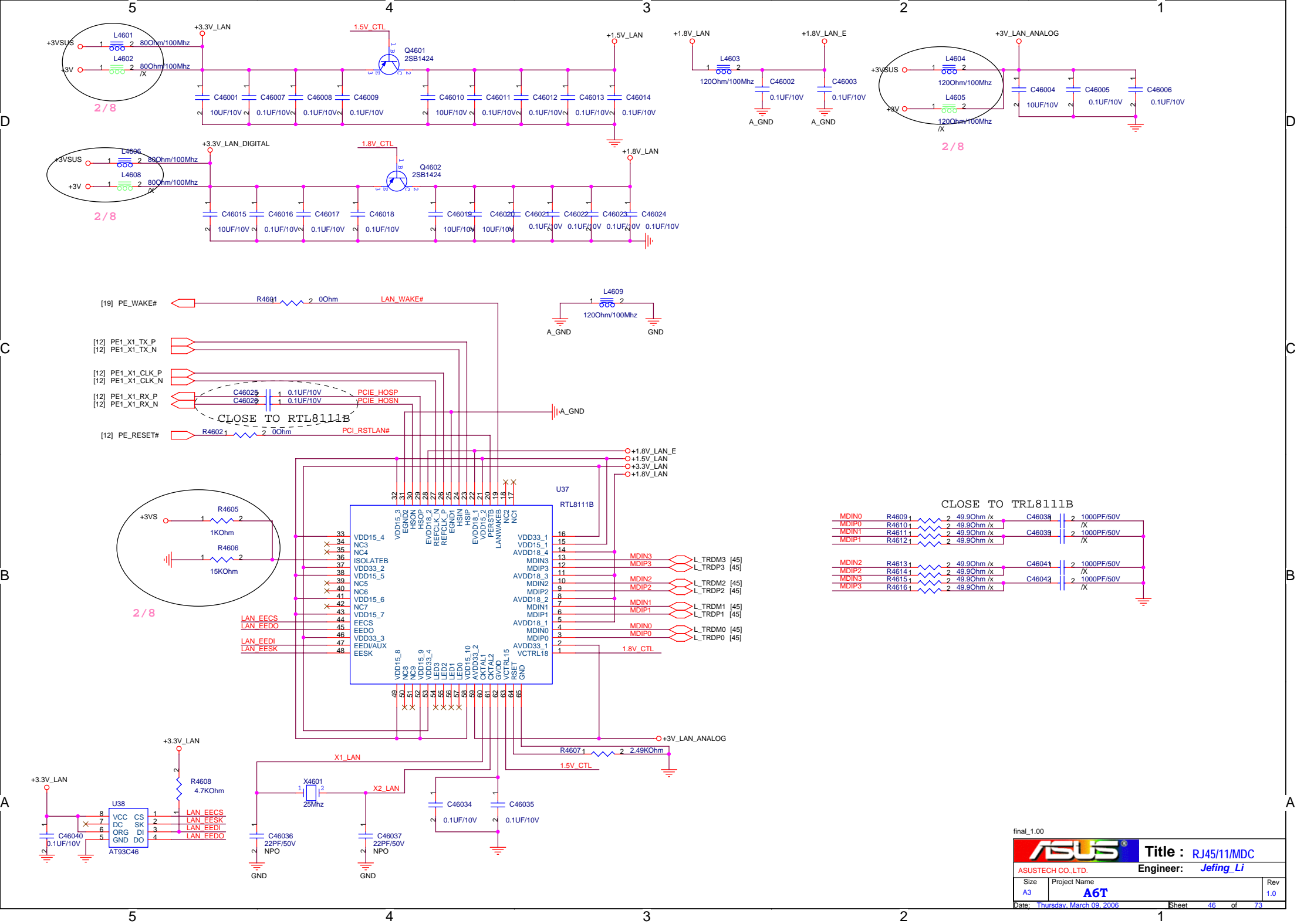
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



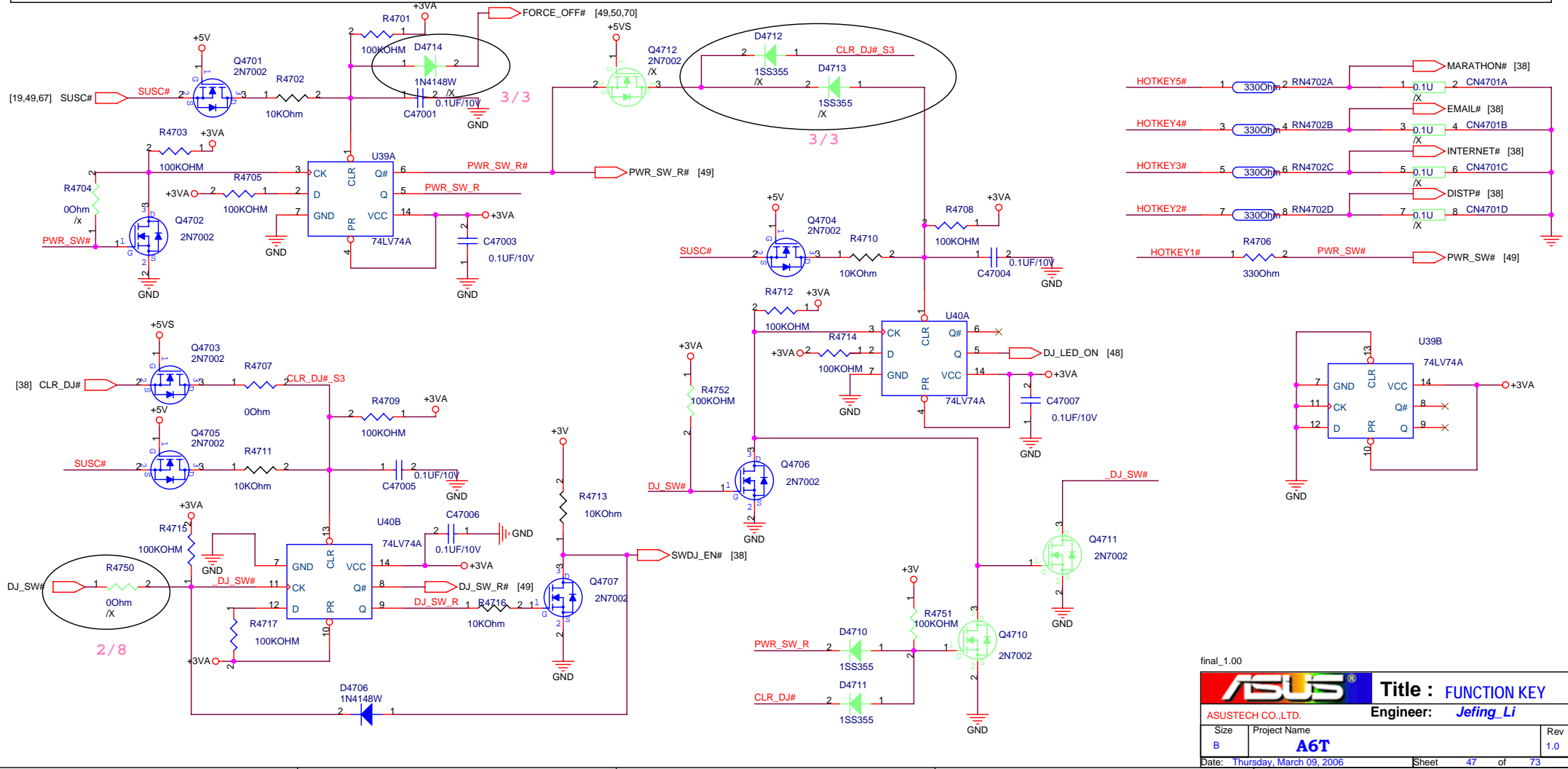
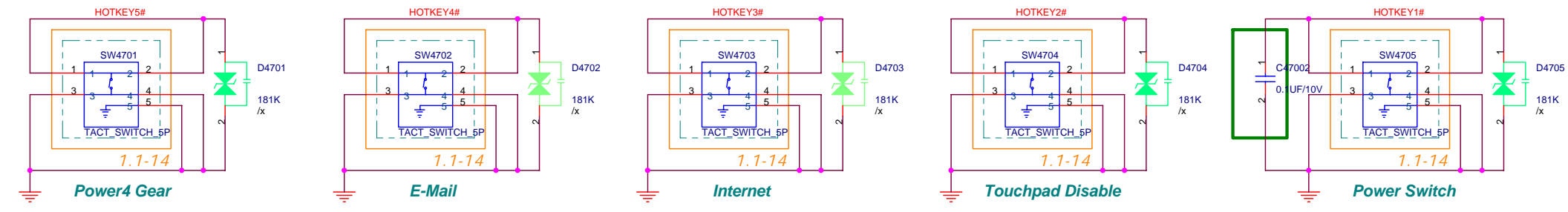


MDC



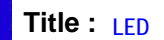


FUNCTION KEY



final_1.00

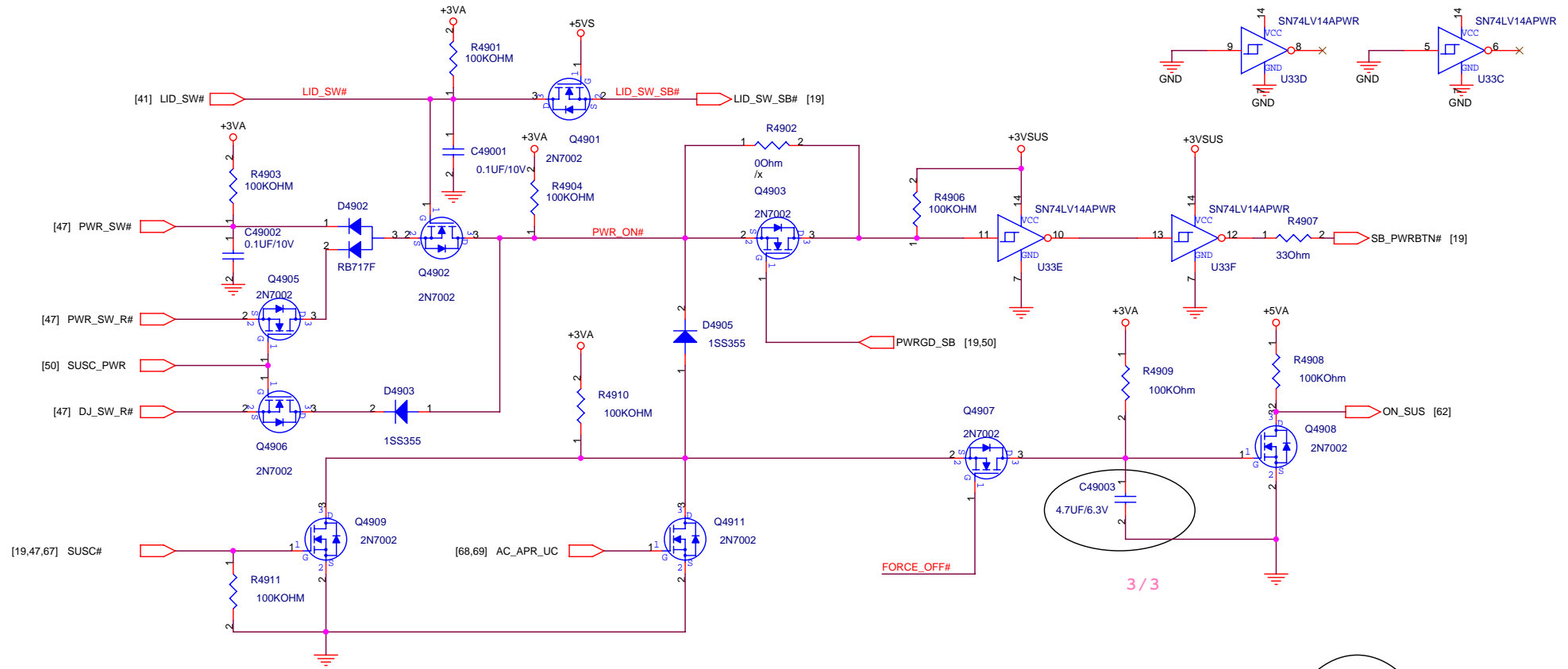
ASUS		Title : FUNCTION KEY	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size B	Project Name A6T		Rev 1.0
Date: Thursday, March 09, 2006		Sheet 47 of 73	



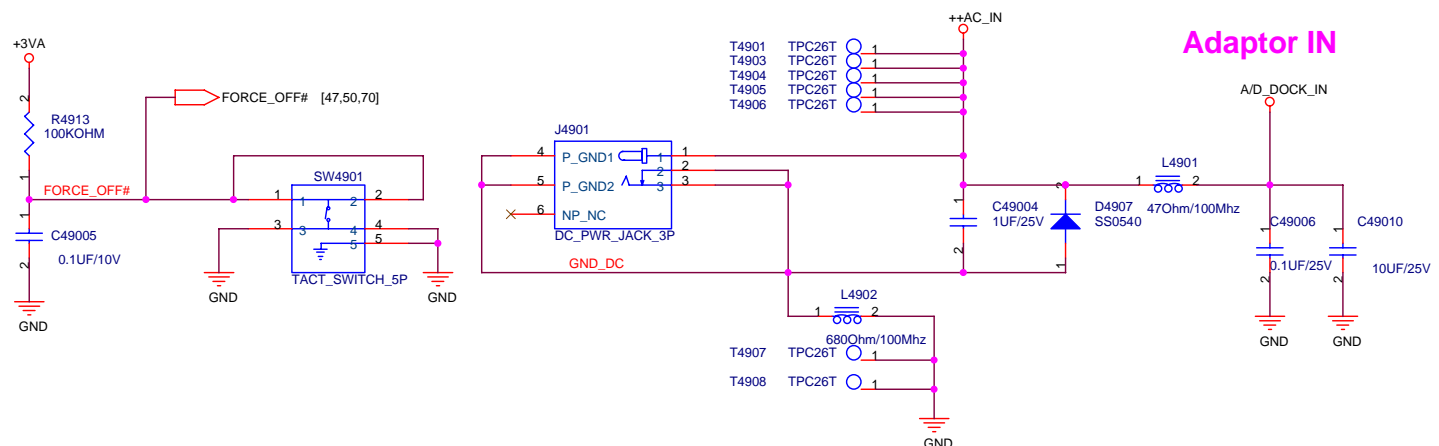
ASUSTECH CO.,LTD.

Engineer: *Jefing_Li*

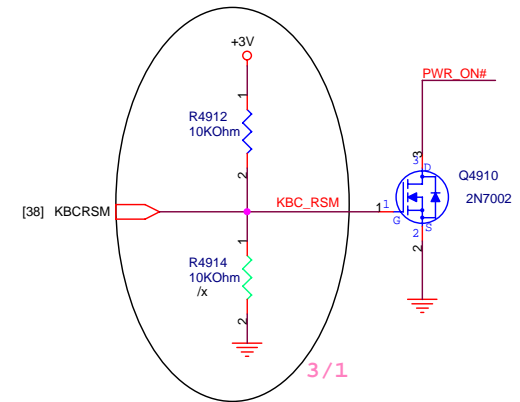
Size B	Project Name A6T	Rev 1.0
Date: Thursday, March 09, 2006		Sheet 48 of 73



3 / 3



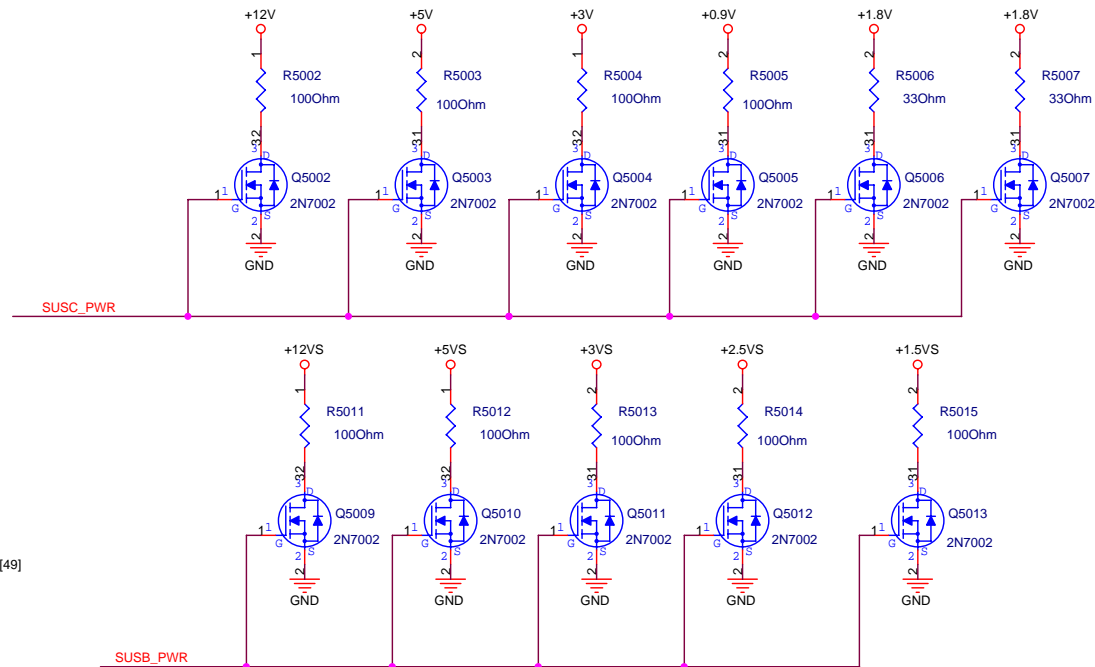
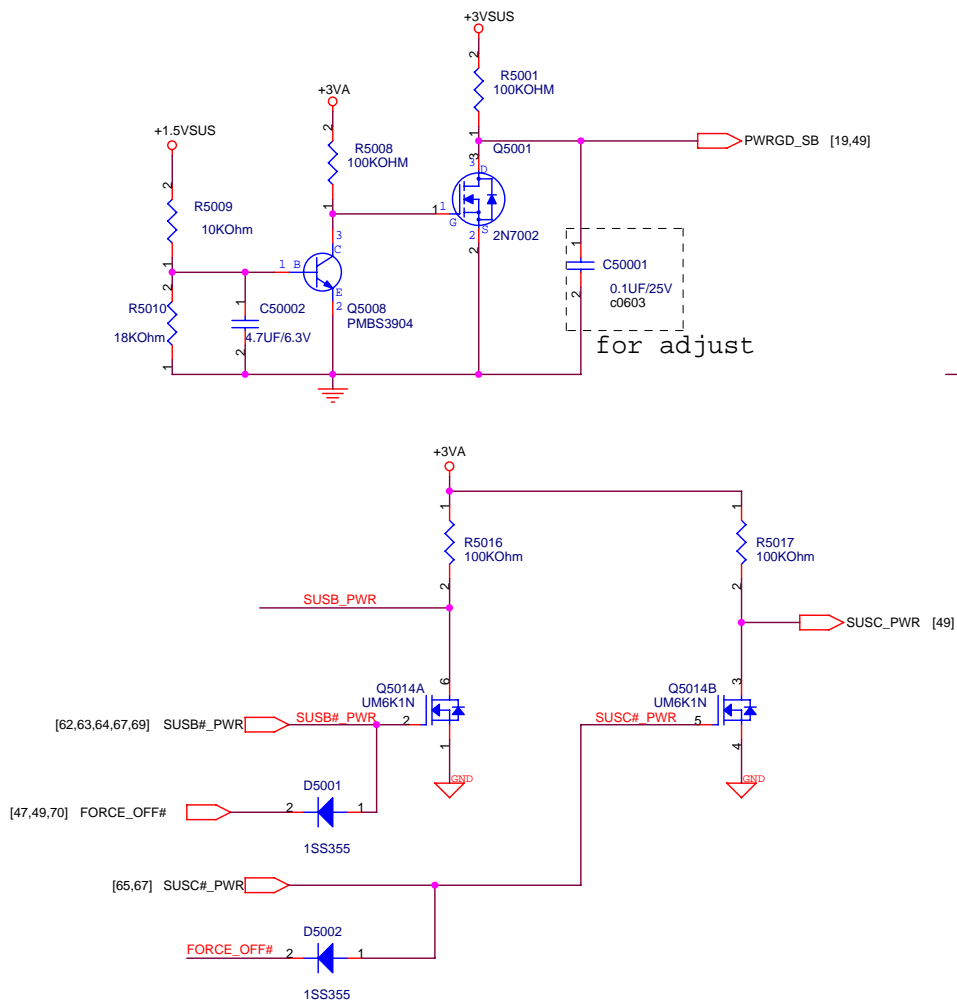
Adaptor IN



3 / 1

final_1.00

ASUS		Title :POWER SEQUENCE(1)	
ASUSTECH CO.,LTD.		Engineer: <i>Jefeng_Li</i>	
Size B	Project Name A6T		Rev 1.0
Date: Thursday, March 09, 2006		Sheet 49	of 73



final_1.00

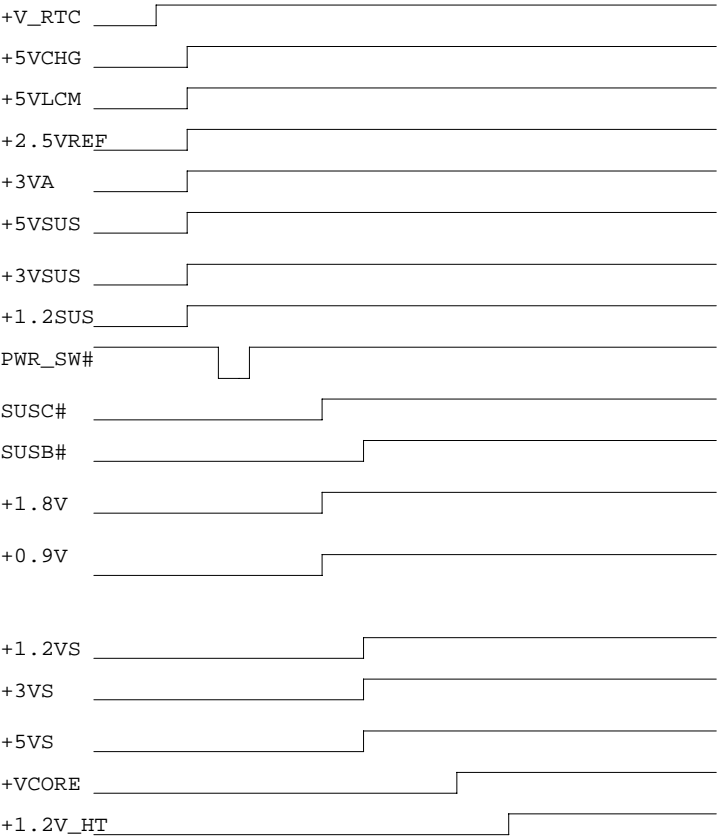
ASUS		Title : POWER SEQUENCE(2)	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size B	Project Name A6T		Rev 1.0
Date: Thursday, March 09, 2006		Sheet	50 of 73

RUN S0-S1 This voltage rail is present when the system is "running"

SUS S0-S1-S3 This voltage rail is present when the system is running or in suspend-to-RAM

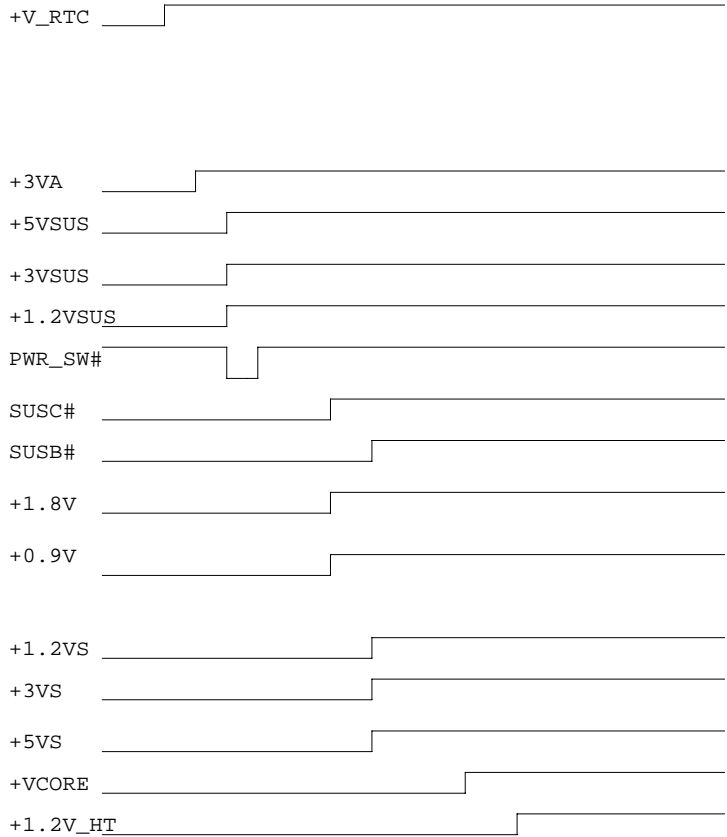
ALWAYS S0-S1-S3-S4-S5 This voltage rail is always present as long as there is main power, whether in the form of a system battery, an AC adapter, or other type of main power supply

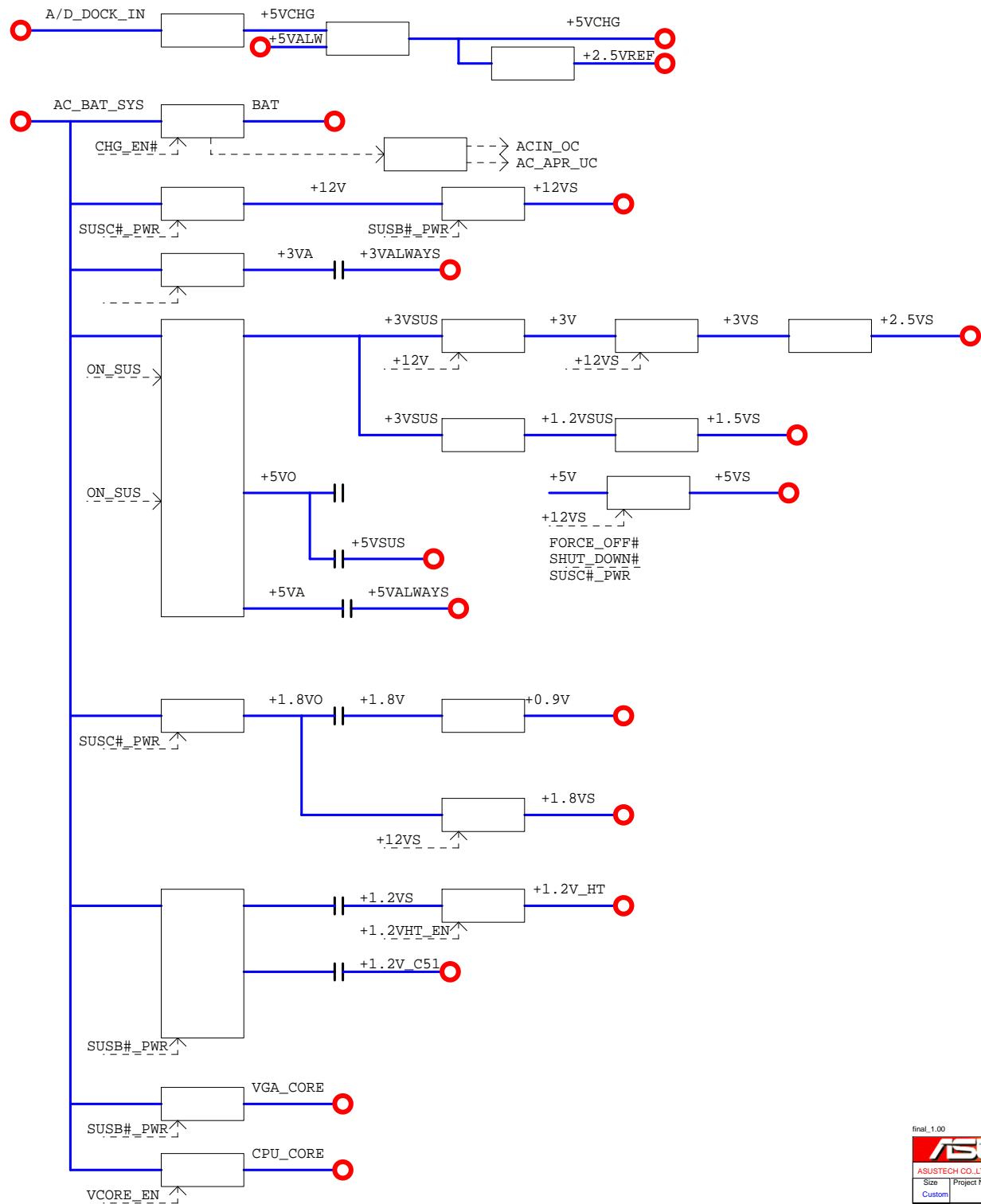
AC MODE



RTC S0-S5, G3 This voltage rail is always present for the Real Time Clock and CMOS RAM circuitry even in the mechanical off state as long as the coin cell is present and not discharged.

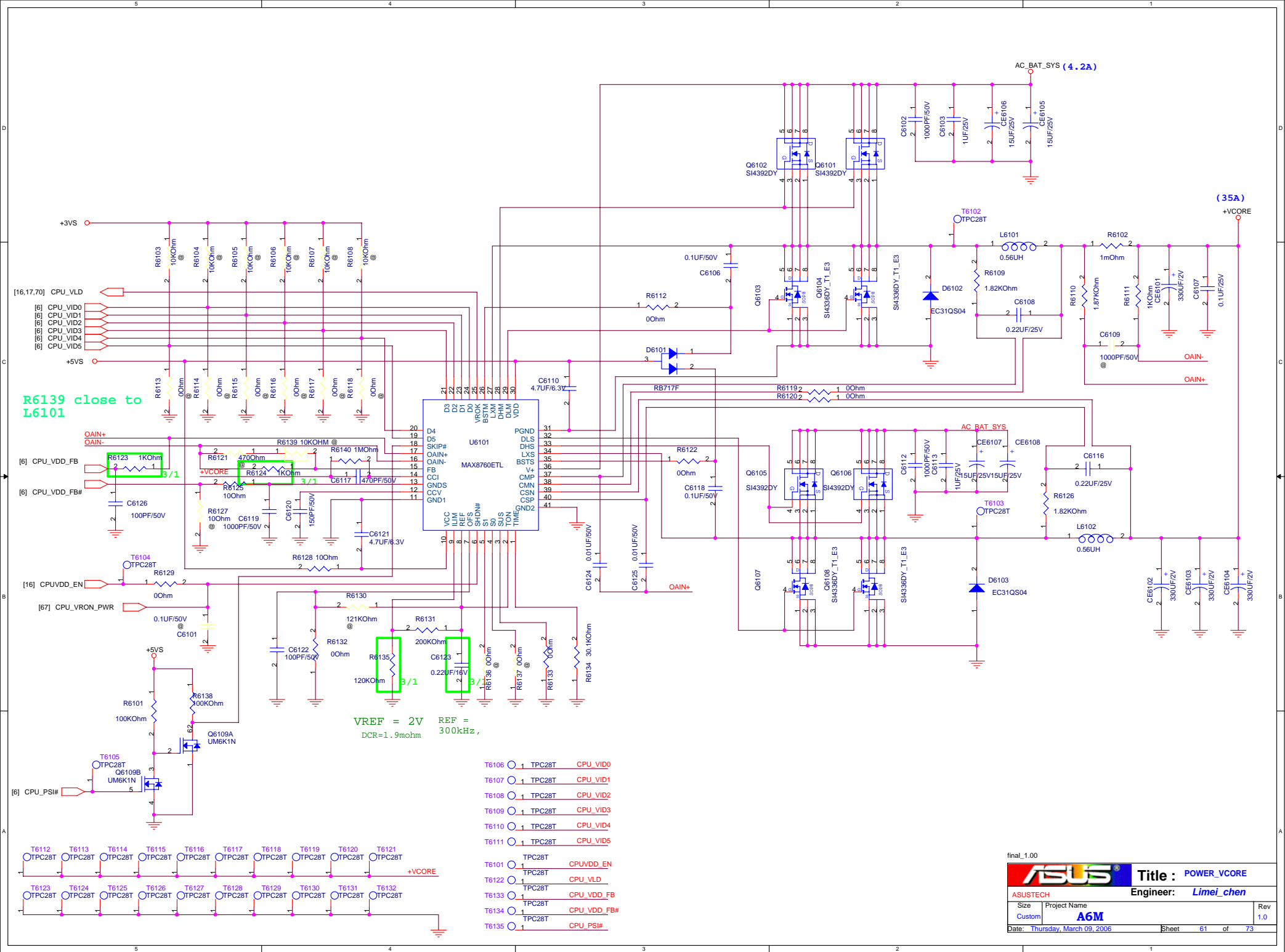
BAT MODE





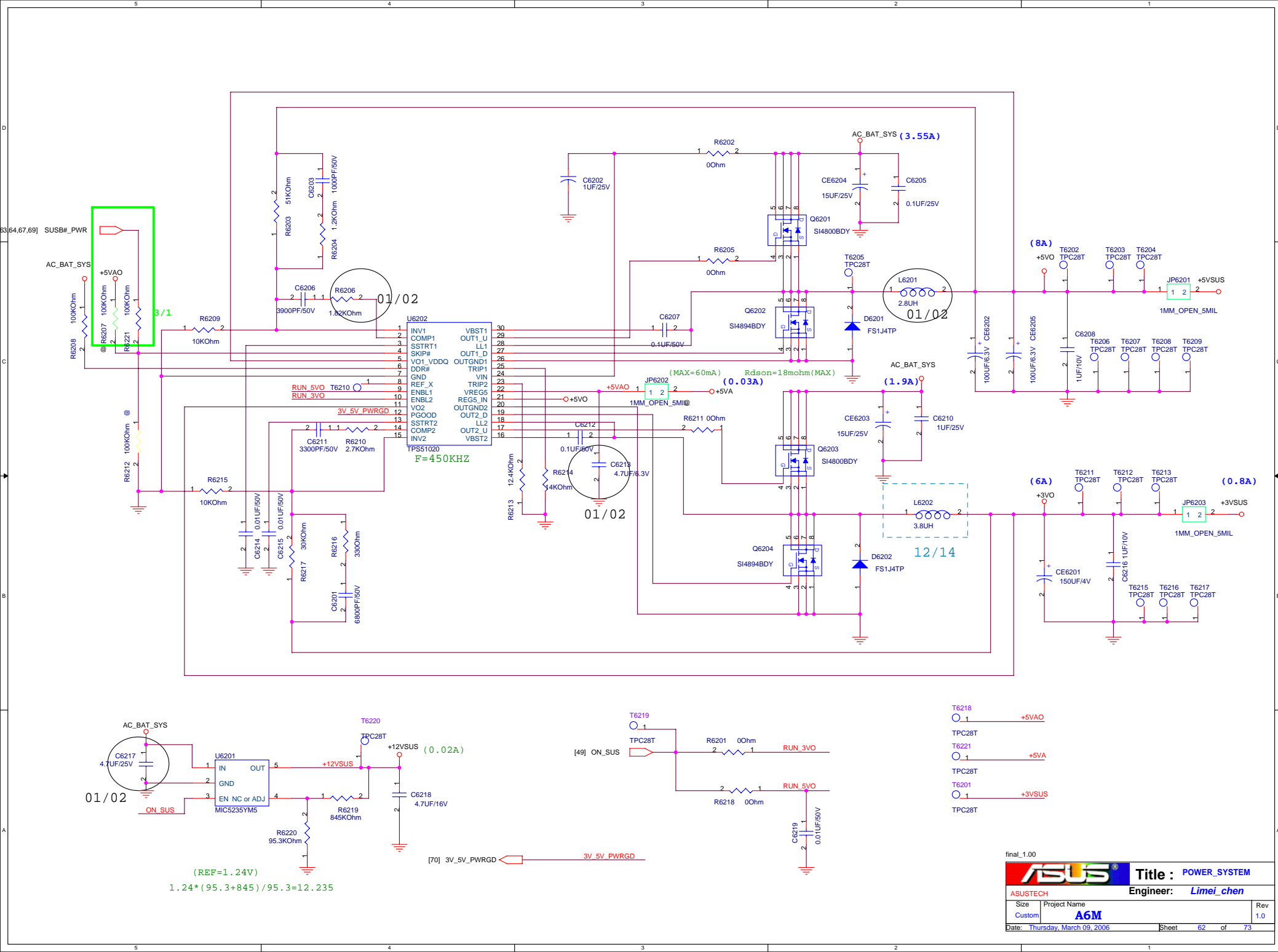
final_1.00

ASUS		Title : POWER BUDGET BLOCK	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name	Rev	
Custom	A6T	1.0	
Date: Monday, March 06, 2006		Sheet 53 of 73	

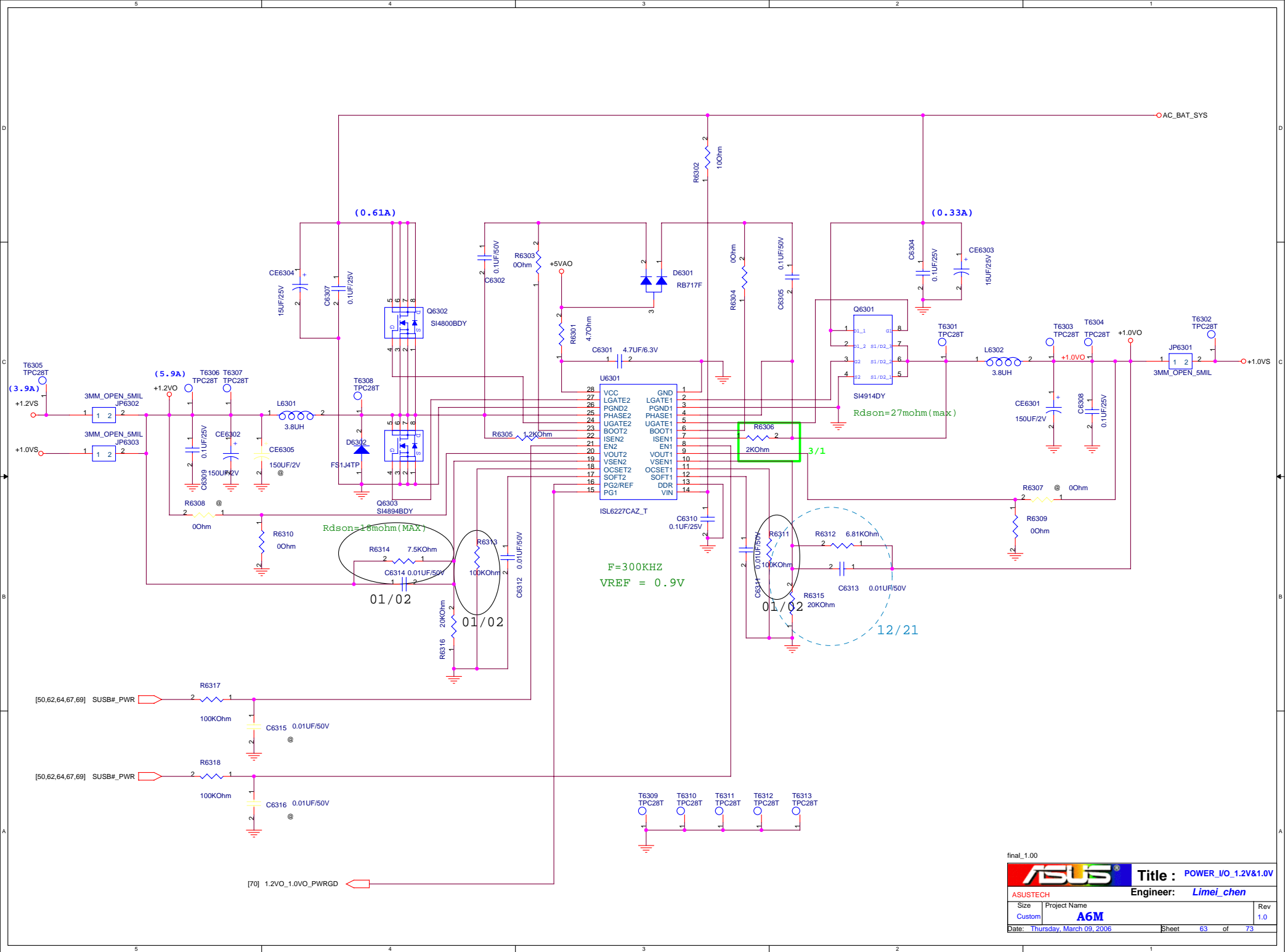


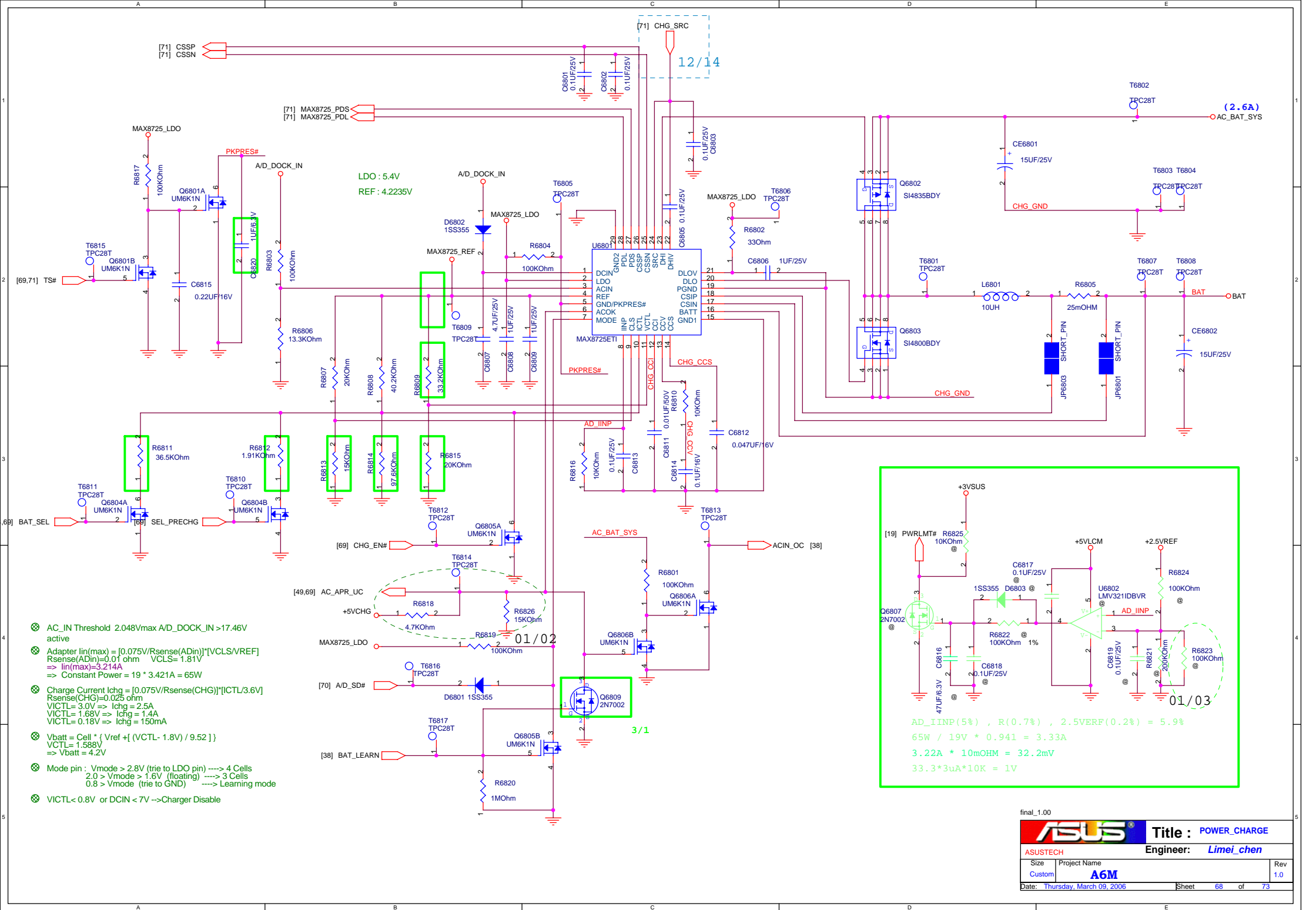
final_1.00

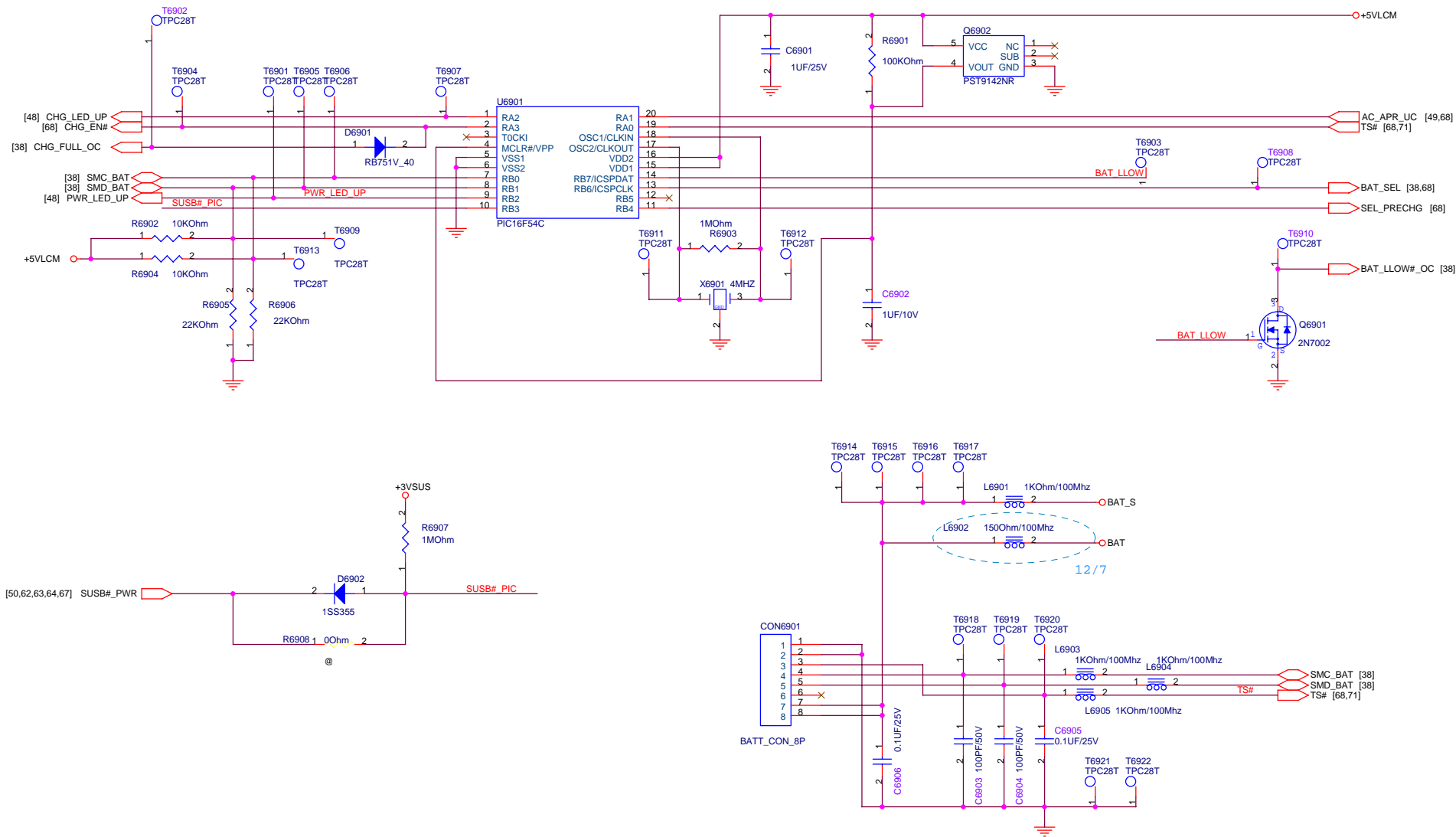
ASUS		Title : POWER_VCORE	
ASUSTECH		Engineer: Limei_chen	
Size	Project Name	Rev	
Custom	A6M	1.0	
Date: Thursday, March 09, 2006		Sheet 61 of 73	



(REF=1.24V)
 $1.24 * (95.3 + 845) / 95.3 = 12.235$

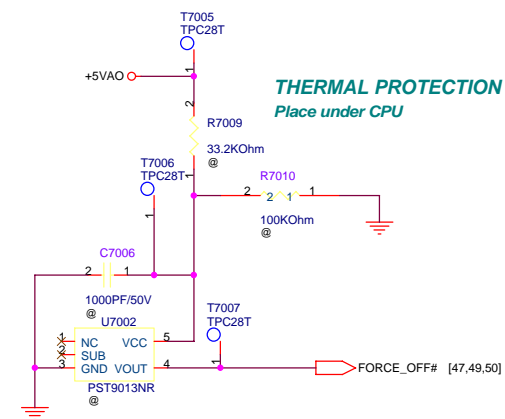
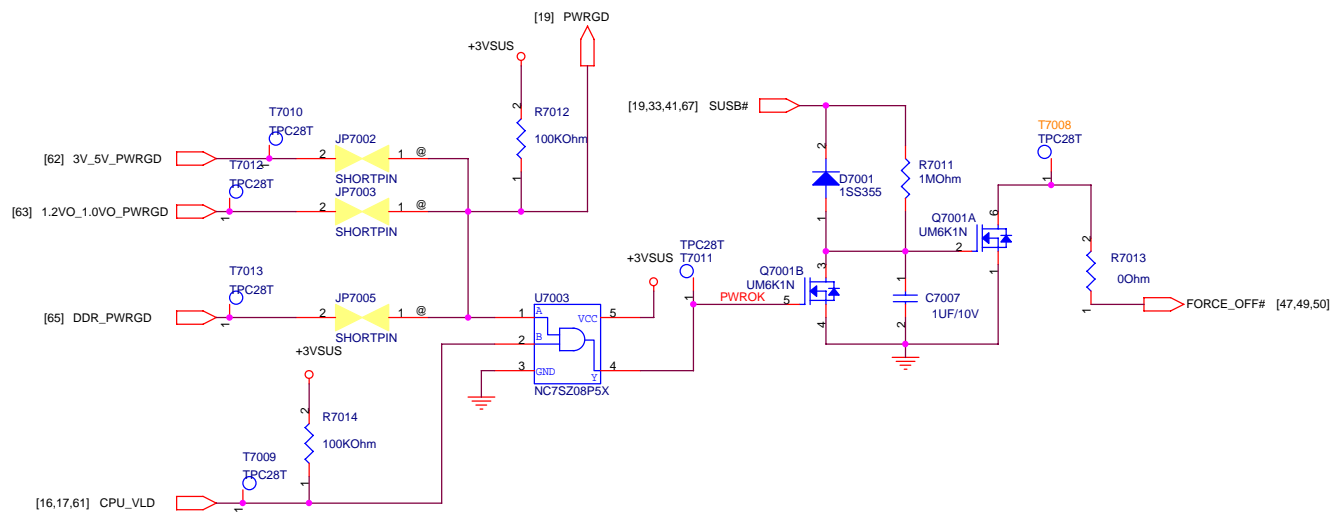
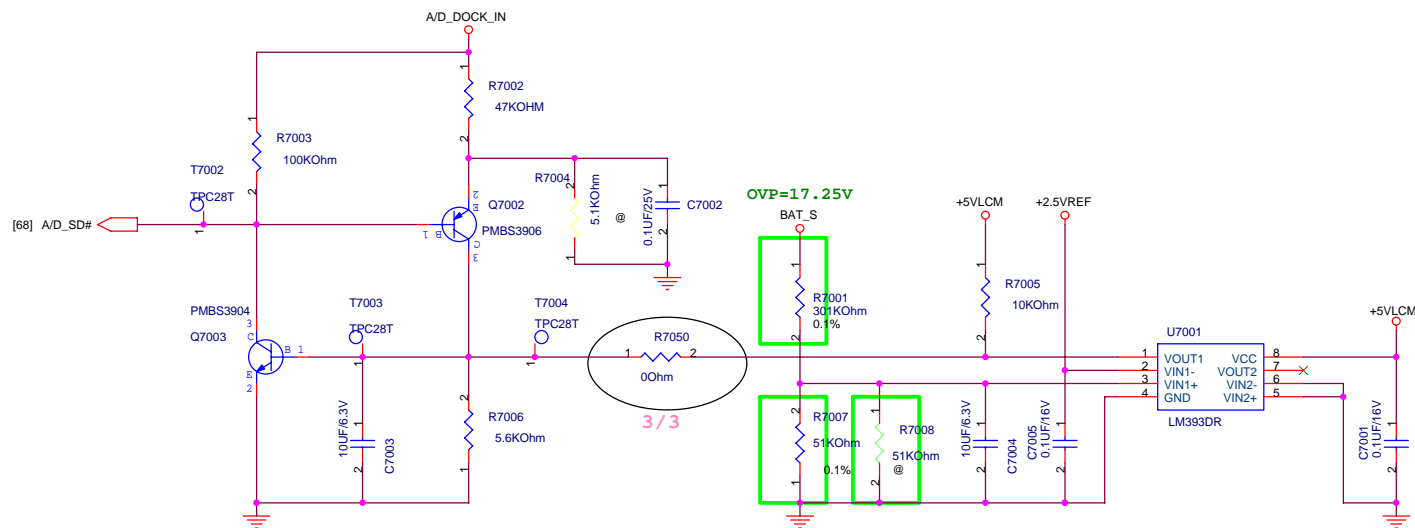


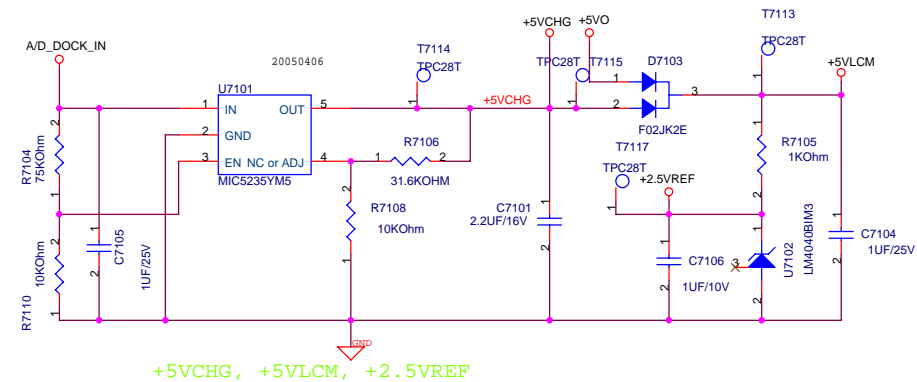
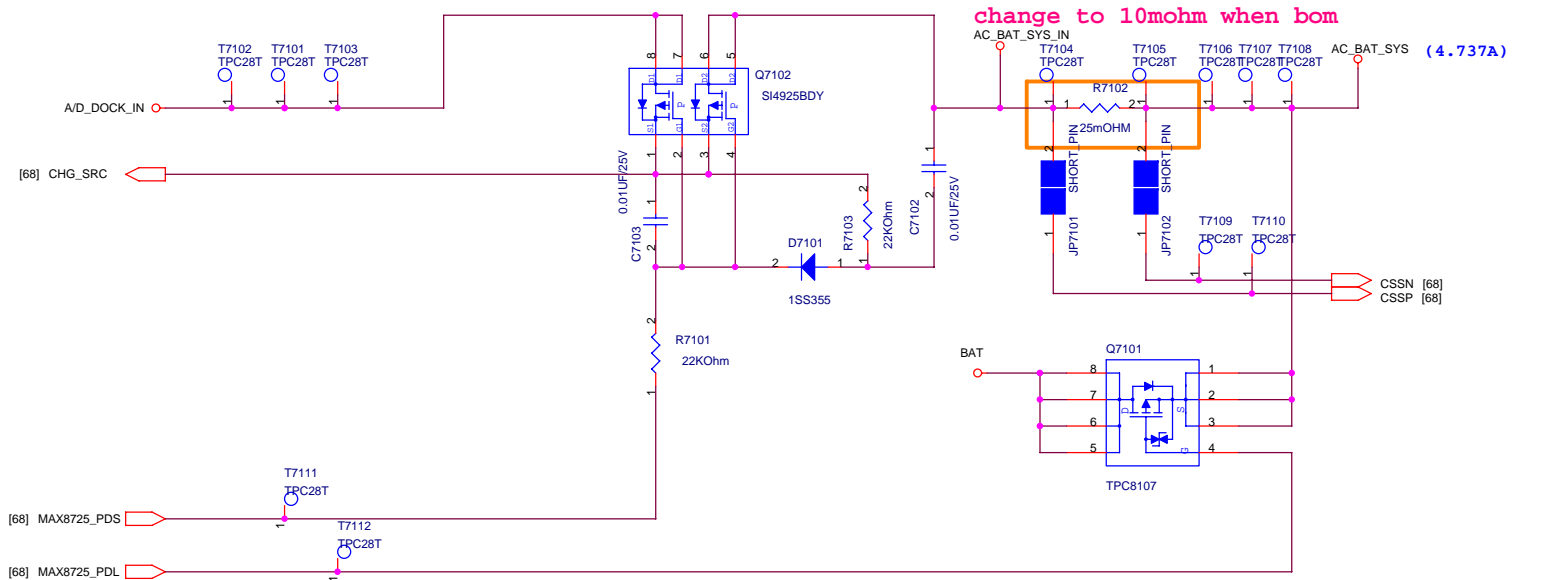




final_1.00

ASUS		Title : POWER_PIC	
ASUSTECH		Engineer: Limei_chen	
Size	Project Name	Rev	
Custom	A6M	1.0	
Date: Thursday, March 09, 2006		Sheet 69 of 73	



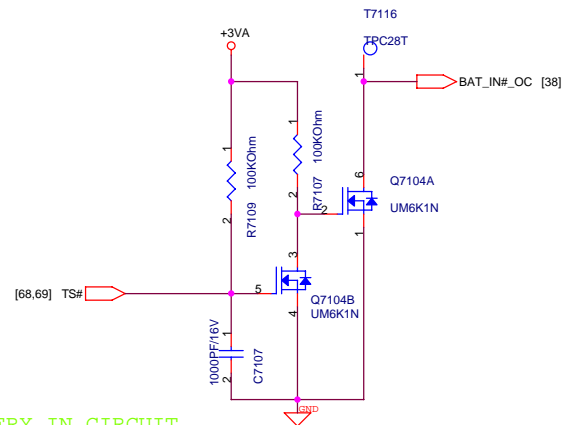


Ref: 1.24V

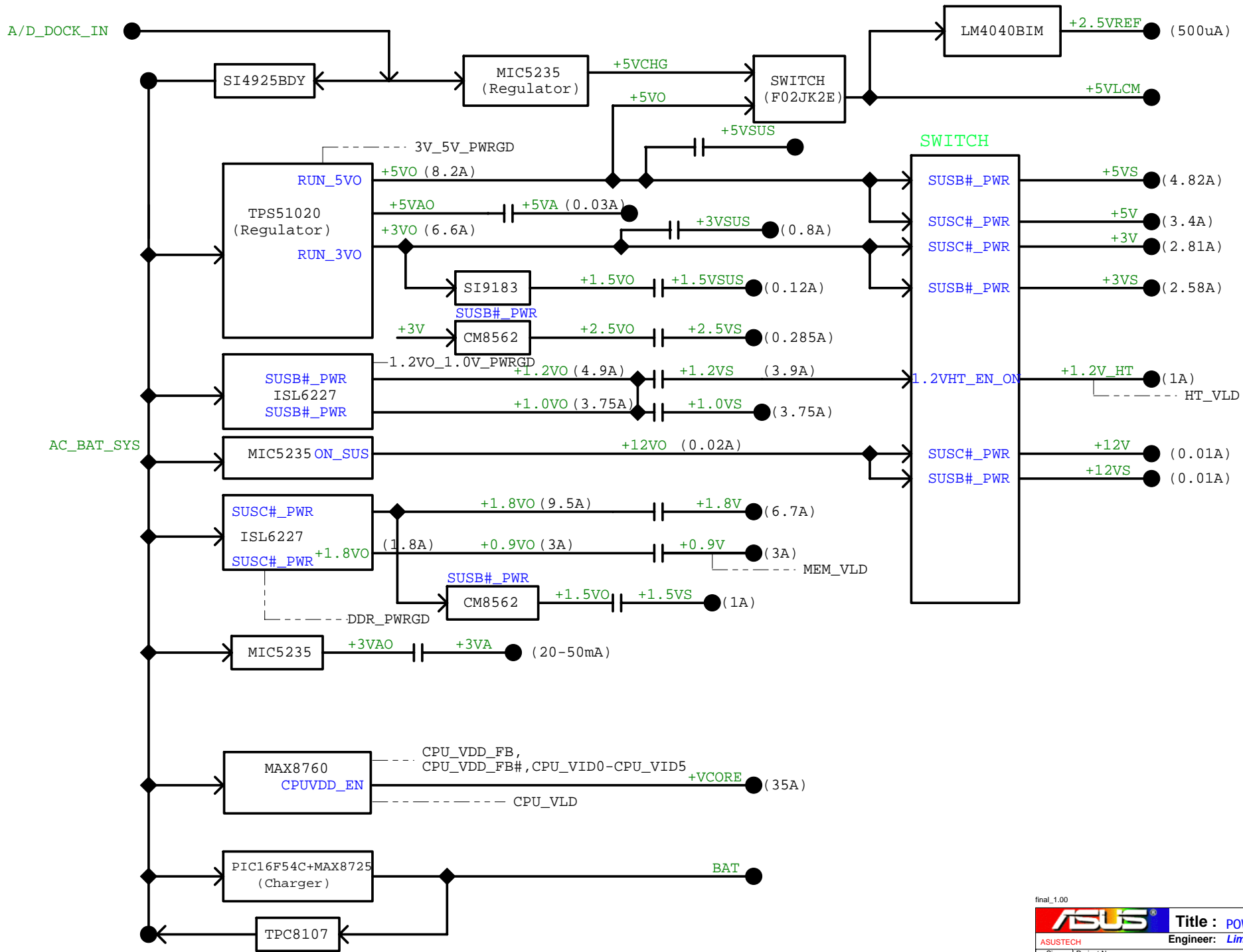
ON: EN>2V (A/D_DOCK_IN:17V)

OFF: EN<0.6V (A/D_DOCK_IN:5.1V)

BATTERY IN CIRCUIT



final_1.00



final_1.00

1206_1

Add Page 73

Page19, add I2C_CLK0_S,I2C_DATA0_S, pull up to +3vs
Page38, remove R3811
Page46, change +3V_LAN to +3.3V_LAN
Page46, remove Q4603
Page19,42. modify AC97 link serial termination. and
place the resistor at the right location.